ELECTRONIC AND STRUCTURAL PROPERTIES OF PENTACENE AT ORGANIC/INORGANIC INTERFACES

by

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Abstract

Organic/inorganic interfaces play a crucial role in flexible electronic devices such as organic field effect transistors (OFETs), organic light emitting diodes (OLEDs) and organic photovoltaics (OPVs). Charge injection and transport through the interface is not only important in understanding devices, but also a primary challenge in developing and optimizing devices. More flexibility in fabricating and controlling devices can be obtained through modifying inorganic surfaces using functional molecules. Functionalized interfaces can be incorporated into OFETs and probed using current-voltage characteristics. This thesis outlines how organic/inorganic interfaces can be studied electrically in OFETs and demonstrates how this strategy can be utilized to characterize tailored interfaces with nanometer-scaled layers.

In this thesis, we studied the interface between organic semiconductors and SiO_2 using structural and electrical characterization of pentacene monolayers on SiO_2. The dependence of the electrical properties of pentacene on the structure of pentacene islands was studied using atomic force microscopy and *in situ* electrical measurements during deposition. The mobilities of holes in pentacene monolayers were extracted using four-contact electrical measurements that probe the pentacene layer independent of the metal-pentacene contacts.

We studied the electrical properties of rubrene thin films deposited on SiO_2 and polystyrene. Rubrene thin film transistors showed very low field effect mobilities on SiO_2. Enhanced mobilities on polystyrene were related to the structural properties of rubrene at the interface between rubrene and the gate dielectrics. Both electron and hole conduction

was observed in the devices.

The interaction between charge carriers in pentacene and a functionalized gate dielectric surface can be studied using the current-voltage characteristics of OFETs. DR19 and C_{60} molecules were attached to the SiO_2 surface. Electrical characteristics of pentacene deposited on these modified surfaces were linked to a change in the electronic structure of the interface. Inserting the functional layers between pentacene and SiO_2 provided photoresponsive characteristics that can be quantified in terms of device parameters in OFETs. These OFETs can be adopted as test structures for studies of the charge transfer at interfaces.

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Table of Contents

Abstract……………………………………………………………………………….….. i

Acknowledgments ………………………………………………………………….....iii

Chapter 1: Introduction ……………………………………………………………….1
1.1 Organic/inorganic interfaces in organic electronics ………………………………....1
1.2 Organic field effect transistors (OFETs)……………………………………….....…4
1.2.1 Device operations………………………………………………………………..5
1.2.2 Device fabrication……………………………………………………………..9
1.3 Physics of organic semiconductors…………………………………………….....10
1.3.1 Introduction………………………………………………………...…....10
1.3.2 Organic semiconductors………………………………………………….11
1.3.2.1 Pentacene…………………………………………………………12
1.3.2.2 Rubrene………………………………………………………....13
1.3.2.3 C_{60}……………………………………………………………...15
1.4 References……………………………………………………………………15

Chapter 2: Channel Formation in Single-Monolayer Pentacene Thin Film Transistors…..21
2.1 Introduction ………………………………………………………………….21
2.2 Experimental methods……………………………………………………….25
2.3 Percolation of pentacene islands on SiO_2 ……………………………………....27
2.4 Electrical and structural properties of monolayer pentacene on SiO_2……………..31
2.5 Contact resistance in monolayer transistors………………………………………..35
2.6 Conclusions……………………………………………………………………...40
2.7 References………………………………………………………………………41

Chapter 3: Orientation of Pentacene molecules on SiO_2…………………………………44
3.1 Introduction ……………………………………………………………………..44
3.2 Experimental methods …………………………………………………………..45
3.3 Polarization-dependent NEXAFS and molecular orientation ……………………..46
3.4 Molecular orientation of pentacene on SiO_2……………………………………49
3.4.1 Effect of thickness on molecular orientation………………………………..49
3.4.2 Effect of deposition rate on molecular orientation…………………………51
3.5 Conclusions ……………………………………………………………………..55
3.6 References………………………………………………………………………56

Chapter 4: Functional Self-Assembled Monolayers for Large Photoinduced Charge Transfer in OFETs………………………………………………………………………57

4.1 Introduction ……………………………………………………………………..57
4.2 Experimental methods…………………………………………………………...59
4.3 Threshold voltage shifts by dipole field effect……………………………………..62
4.4 Threshold voltage shifts due to photoinduced charge transfer……………………..66
4.5 Light intensity effect on threshold voltage shifts…………………………………..70
4.6 Gate electric field effect on threshold voltage shifts………………………………72
4.7 Reversibility of photoinduced charge transfer……………………………………...76
4.8 Growth of pentacene on functionalized surfaces…………………………………..78
4.9 Conclusions………………………………………………………………………...80
4.10 References…………………………………………………………………...…80

Chapter 5: Self-Assembled Dipolar Chromophores in OFETs………………………83
5.1 Introduction ……………………………………………………………………..83
5.2 Experimental methods …………………………………………………………..83
5.3 Structural characterization of DR19 on SiO_2 surface……..………………………...84
5.4 Threshold voltage shifts in FETs…………………………………………………...85
5.5 Effect of the light intensity on the threshold voltage shifts……………………...…87
5.6 Effect of gate electric field on threshold voltage shifts……………………...…..88
5.7 Effect of the DR19 thickness on threshold voltage…………………………...…89
5.8 Structural changes in DR19 under illumination…………………………………..91
5.9 Photoinduced charge transfer between DR19 and pentacene………………………94
5.10 Conclusions………………………………………………………………….…95
5.11 References………………………………………………………………….....95

Chapter 6: Rubrene Ambipolar Thin Film Transistors……………………………………97
6.1 Introduction…………………………………………………………………………...97
6.2 Experimental methods…………………………………………………………...98
6.2.1 Structural identification of rubrene using FT-IR…………………………....98
6.2.2 3D growth of rubrene on SiO_2……………………………………………99
6.2.3 Molecular orientation of rubrene on SiO_2…………………………………101
6.3 Electrical properties of rubrene thin Films………………………………………102
6.3.1 Channel formation in rubrene thin film transistors………………………102
6.3.2 Ambipolar charge transport in rubrene Thin Films………………………105
6.4 Conclusions……………………………………………………………………110
6.5 References……………………………………………………………………...110

Chapter 7: Enhanced Hole Mobility in Ambipolar Rubrene Thin Film Transistors on Polystyrene……………………………………………………………………………113
7.1 Introduction……………………………………………………………………113
7.2 Experimental methods…………………………………………………………114
7.3 Growth of rubrene on polystrene……………………………………………116

7.4 Electrical properties of rubrene on polystyrene……………………………………117
7.5 Ambipolar characteristics of rubrene transistors……………………………………119
7.6 Conclusions…………………………………………………………………..121
7.7 References…………………………………………………………………121

Chapter 1

Introduction

1.1 Organic/inorganic interfaces in organic electronics

Organic electronics have been aggressively studied for applications in electronic displays, sensors, radio frequency identification tags, smart cards and organic solar cells [1]. This large range of possible applications can be realized by understanding the basic science in involved in the operation of organic electronic devices and the physics of organic semiconductors.

Interfaces in organic electronic devices such as organic field effect transistors (OFETs), organic light emitting diodes (OLEDs) and organic photovoltaics (OPVs) take part in charge injection and transfer which are crucial for operating devices. For example, the cathode and anode layers form contacts to an electron transport and hole transport layer [2-6]. The alignment of molecular energy levels between the electrodes and the transport layers can be tuned by attaching self assembled monolayers (SAMs) to the metal electrodes. The SAMs can alter the electrostatic potentials at the interface between metal and organic semiconductors and thus control the injection barrier to the organic semiconductors [7-10].

Photoinduced charge transfer between electron acceptor and donor layers is critical in determining power conversion efficiency in OPVs [11-13]. In these devices, the absorption of light produces excitons in the electron donor layer that are subsequently dissociated at

the interface. For efficient charge transfer at the interface, an intimate contact between donor materials with a low ionization potential and acceptor materials with a high electron affinity is required.

In OFETs, charge injection between the metal electrodes and the organic semiconductor and charge transport along the interface between gate dielectric and organic layers are the most important processes in the operations of these devices [14, 15]. For example, the choice of metal electrodes can change the contact resistance between the metal electrodes and organic semiconductors. In order to achieve efficient charge injection from metal electrodes to p-type organic semiconductor, metal electrodes with high work function are required. For efficient electron injection metal electrodes with low work function are desired [16, 17].

It has been reported that the contact resistance between metal electrodes and organic semiconductors can affect the mobility of charge carriers in organic semiconductors in OFETs [16, 18-19]. In the literatures, higher FET mobilities were obtained in devices by lowering contact resistance.

The gate dielectric can affect transport carriers in organic semiconductors. When an electric field is applied across the gate dielectric charge carriers are induced near the gate dielectric. The induced charges form a two dimensional conducting channel near the gate dielectric rather than traveling in the three dimensional bulk. The interface states between organic semiconductors and the gate dielectric can act as trap sites for charge carriers resulting in the change of the device parameters such as threshold voltage and on/off ratio [20].

In addition, the surface properties of the gate dielectric can affect the structure of the films grown on the gate dielectric by changing the interactions between organic molecules and the gate dielectric [21]. The roughness of the gate dielectric can also change the morphology of the organic film. The increased roughness of the gate dielectric can produce valleys in the electrical channel between source and drain electrodes, which is undesirable for transport of carriers at the interface between the gate dielectric and the organic layer. The nucleation density of organic semiconductors depends on the surface properties of the gate dielectric. This nucleation density changes the grain size of organic films deposited on gate dielectrics. For example, the grain size of pentacene on the Si surface treated with cyclohexene was much larger than on Si surface without any treatments [21]. A larger grain size has been linked to a higher mobility of carriers in organic semiconductors by reducing grain boundary which can trap the carriers.

Tailoring the interfaces of organic electronic devices can not only optimize the device performance but also provides more flexibility in designing device structures. The interfaces can be functionalized and incorporated in a variety of electronic devices [22, 23]. In OFETs, the surface properties of the gate dielectric have been modified with self assembled monolayers (SAMs) such as hexamethyldisilazene (HMDS) and silanes including octadecyltrichlorosilane (OTS) [20, 24-26]. The mobilities of carriers in organic semiconductors on the modified surfaces were improved. The origin of the improved mobility, however, is not well understood. It has been argued that increased grain size of pentacene using gate dielectric functionalized with silanes contributed to the improved mobility [27]. The molecules covalently attached to the inorganic gate dielectrics may

change the surface energy. The surface energy of silanized surfaces was reduced and the larger grain size of pentacene was reported [26].

Functionalizing the gate dielectric with a built-in dipole changes the threshold voltages of OFET devices [28, 29]. Charge carrier densities in the conducting channel depend on the magnitude of the dipole moment of SAMs attached to the gate dielectric. In OFETs and OLEDs, the work function of metal electrodes can be tuned by functionalizing metal electrodes with polar molecules. Alkanethiols attached to metal electrodes reduce the work function of metal electrodes and perfluorinated alkanethiols with opposite dipole increase the work function of metals [30-34].

1.2 Organic field effect transistors (OFETs)

The discovery of electrical conductivity in polymers enabled the production of organic electronic devices such as OFETs, OLEDs and OPVs. OFETs were first reported in 1986 and since then many advances in device performance have been made [35, 36]. The possibility of printing flexible electronic devices using OFETs has stimulated research devoted to discovering organic semiconductors with high conductivity and to optimizing device performance [14, 37-38].

The structures of OFETs are shown in Fig. 1.1(a). A gate dielectric layer separates the gate electrode from the organic semiconductor layer. In the bottom-contact geometry, source and drain electrodes are formed on the gate dielectric and are used as contacts to the organic semiconductor. OFETs are operated in accumulation mode in which the electric field applied between the gate and the organic semiconductors attracts charge carriers into

a very thin sheet of charge at the interface between the organic semiconductor and the gate dielectric [2, 39]. The capacitance of the gate dielectric determines the charge density that can be induced in the organic active layer by applying a voltage between the gate and the semiconductor. This effect is illustrated in Fig. 1.1(b). Applying a negative voltage to the gate increases the fermi energy level (E_F) and this leads to energy band bending at the interface between the gate dielectric and the organic semiconductor. E_C, E_V and E_i represent conduction band, valence band edge and intrinsic energy level, respectively.

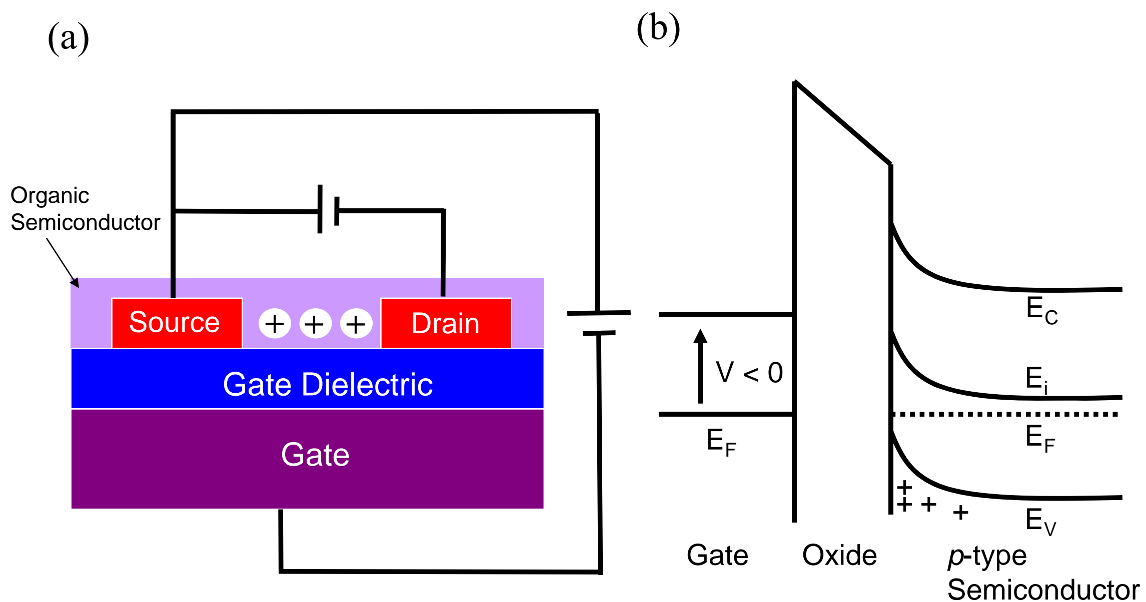

Fig. 1.1: Schematic diagrams of a) the FET geometry and (b) FET operation in accumulation mode

1.2.1 Device operation

It is important to understand the device physics of OFETs in order to use OFETs as tools for probing charge transport in organic semiconductors. Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) theory has been used to explain and interpret charge transport phenomena in OFETs [37, 40].

In OFETs, charge carriers at the interface between the gate dielectric and the semiconductor layer are responsible for the conduction through the device. Fig. 1.2(a) shows an energy band diagram for a metal-oxide-semiconductor (MOS) structure at zero gate voltage. In this flat band condition, no band bending occurs at the interface between the oxide and the semiconductor. When the gate voltage is changed to the flat band voltage (V_{FB}), flat band condition is achieved. In Fig. 1.2, the flat band voltage is 0 V. When a negative gate voltage is applied to the gate, holes accumulate in the organic semiconductor, as in Fig. 1.2(b).

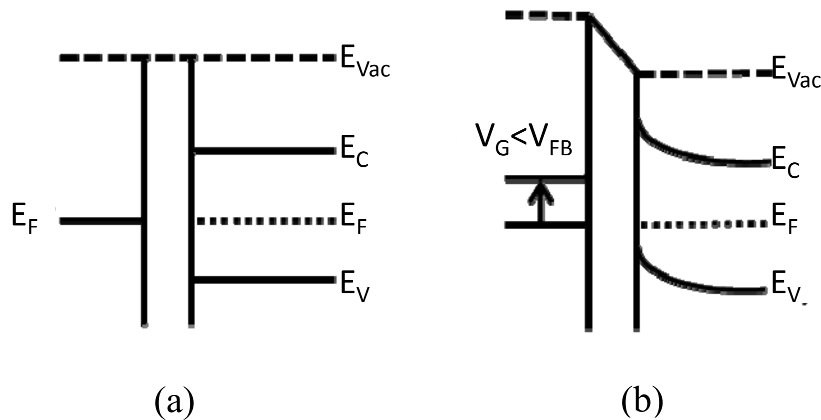

Fig. 1.2: Energy band diagrams for a metal-insulator-semiconductor transistor based on a p-type semiconductor. (a) Flat band condition and (b) accumulation of holes when $V_G<V_{FB}$.

A larger negative gate voltage induces more mobile charge carriers in the channel and increases its conductivity. The charge density profile of induced carriers perpendicular to the surface is closely related to the band bending at the interface and number of induced charge carriers. The accumulation layer thickness, Z_{av}, is estimated to be 1-2 nm, which shows OFETs are very sensitive to the interface between the gate dielectric and the semiconductor [2, 39, 41].

The transistor accumulates charges in the semiconductor for gate voltages larger than V_{FB}, as shown in Fig. 1.2(b). Band bending close to the interface arises from these accumulated holes.

Transistors can in general be operated in either of two regimes, the saturation regime and linear regime, differentiated by the relative magnitudes of the source-drain voltage and the gate voltage. When the source-drain voltage is comparable to the gate voltage the channel region near the drain contact begins to be depleted. At this point the voltage difference between gate and drain is equal to threshold voltage, V_T, and the conducting channel is said to be pinched off. In this case the drain current is given by [42]:

$$I_{Dsat} = \frac{W}{2L} \mu C_{gd} (V_G - V_T)^2 \tag{1.2}$$

Here, L and W are the channel length and width, respectively. C_{gd} is the capacitance of the gate dielectric and μ and V_T represent the mobility and threshold voltage, respectively. Threshold voltage is the voltage required to induce mobile charge carriers in the channel. Flat band voltage is the voltage needed to make the vacuum level flat as shown in Fig. 1.2(a). In the MOS structure, flat band voltage is the work function potential difference between metal and semiconductor. Threshold voltage is conventionally thought to be the

flat band voltage in an OFET is operated in accumulation mode.

Transistors operate in the linear regime when the difference between the gate voltage and threshold voltage is much larger than the source-drain voltage. In this regime, I_{Dlin} increases linearly with V_G according to:

$$I_{Dlin} = \frac{W}{L}\mu C_i (V_G - V_T)V_D \tag{1.3}$$

In the linear regime, the conductivity of carriers induced in the channel depends on the charge concentration and the mobility according to the equation.

$$\sigma_{\square} = 1/R_s = ne\mu \tag{1.4}$$

Here, $\sigma_{\square}$ is sheet conductance and n represents two dimensional density of charge carriers. R_s is sheet resistance. In the linear regime, when $V_G > V_T$, the charge carriers induced are mobile and the density can be expressed as:

$$n = \frac{C_{gd}(V_G - V_T)}{e} \tag{1.5}$$

In the linear regime, mobility, μ, can be expressed by:

$$\mu = \frac{\frac{1}{R_s}}{ne} = \frac{1}{C_{gd}} \frac{d\frac{1}{R_s}}{dV_G} \tag{1.6}$$

In equation 1.6, μ was calculated based on the assumption that μ is independent of two dimensional density of mobile carriers induced by V_G. In some cases, the mobility of charge carriers depends on the gate voltage, which is contradictory to the assumption [41, 43]. As gate voltage increases the mobility increases in previously reported literature [44]. This gate voltage dependence of mobility has been predicted by multiple trapping and release (MTR) [45] and charge transport models based on hopping between localized states

[46]. The charge transport mechanism of carriers in organic semiconductors is not entirely clear.

Contact resistance between the metal electrodes and organic semiconductors complicates measurements of mobility. Contacts between metal and semiconductor were assumed to be ohmic in equation 1.3. In MOSFETs, contact resistance can be reduced by doping the semiconductor near the electrodes and the current voltage characteristics in the linear (eq. 1.3) and saturation regime (eq. 1.2) can be widely applied. In OFETs, however, many studies demonstrated that a significant voltage drop is present near the metal-semiconductor contacts [41, 47-48]. In this thesis, we studied how contact resistance can affect the mobility in OFETs.

1.2.2 Device fabrication

Our research used OFETs with the bottom-contact geometry fabricated using photolithography to define source and drain electrodes. A thermally grown 200 nm-thick oxide was used as a substrate (Fig. 1.3(a)). We spincoated an oxidized Si substrate with photoresist (PR) at 4000 rpm for 30 sec (Fig. 1.3(b)). The sample was baked for 2 min at 115°C on a hot plate. The PR was exposed to ultraviolet (UV) light for 12 sec (Fig. 1.3(c)). The chemical structure of the PR exposed to UV was changed and the PR was easily removed by dipping the sample into a developer (MF321) for 3 min (Fig. 1.3(d)). Then, metal layers were deposited by e-beam evaporation (Fig. 1.3(e)). A Cr adhesion layer was deposited on the patterned substrates then a thick Au layer was deposited on the Cr layer.

The metal evaporation was followed by the lift-off process (Fig. 1.3(f)). The sample was dipped in acetone under sonication for 10 min to remove PR.

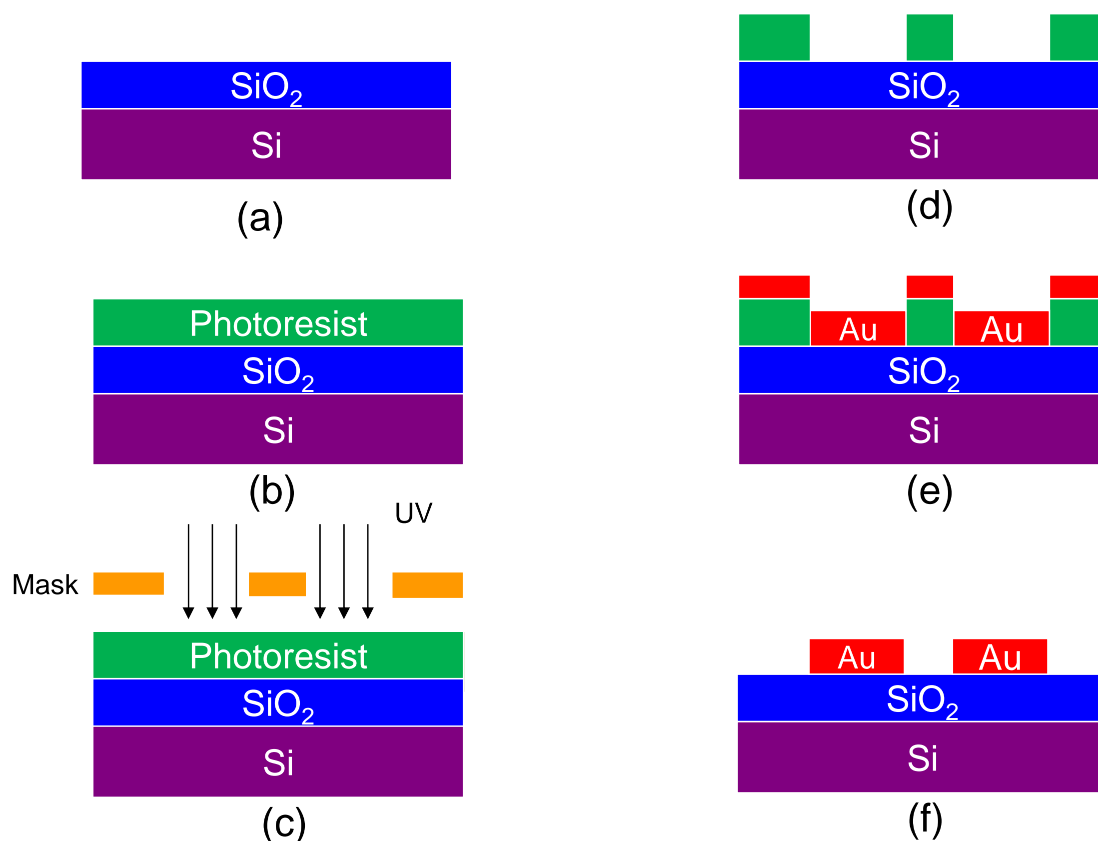

Fig. 1.3: Fabrication steps of a bottom contact-FET device. (a) thermally grown oxide, (b) spinning the PR, (c) patterning and exposing the PR, (d) developing the PR, (e) depositing metal electrodes and (f) removing the PR (lift-off)

1.3 Physics of organic semiconductor

1.3.1 Introduction

Organic semiconductor molecules have conjugated structures with alternating single and

double bonds of carbon-carbon bonds. The molecules have π-orbitals delocalized along the face of a molecule. This orbital delocalization allows electrons to move within a molecule. Organic semiconductors are structurally and chemically quite different from inorganic semiconductors. Inorganic semiconductors consist of atoms that are covalently or ionically bonded. The strong interaction between atoms by covalent boding leads to the delocalization of the individual orbitals of atoms. The interaction between orbitals creates more energy states and forms a quasi-continuous band in which the energy difference between individual energy levels is very small.

In organic semiconductors, molecules are linked to each other by comparatively weak van der waals interactions [38]. Therefore, electrons are largely localized to individual molecules except electrons in the π orbital, and the weak intermolecular interactions cause a narrow electronic bandwidth in molecular solids. The charge transport mechanism in organic semiconductor is not well understood. As the interaction between π orbitals increases the degree of π-π overlap increases. This condition is favorable for the formation of energy bands. Due to the narrow bandwidth arising from the weak interactions between molecules in organic semiconductors the mobilities of charge carriers in organic semiconductors are low, with typical values of 10^{-2} cm^2/Vs, in comparison with values of 100-1000 cm^2/Vs or more in inorganic semiconductors [40, 49-50].

1.3.2 Organic semiconductors

Organic semiconductor can be divided in two groups. Low molecular weight semiconductors based on small organic molecules as in Fig. 1.4, and polymers with higher

molecular weight. Organic semiconductors with low molecular weights can be thermally evaporated and have better crystallinity than polymers. The polymers, however, are processed easily in solution. The weak overlap between molecular orbitals in polymers and semiconductors leads to lower mobility than in small molecule semiconductors.

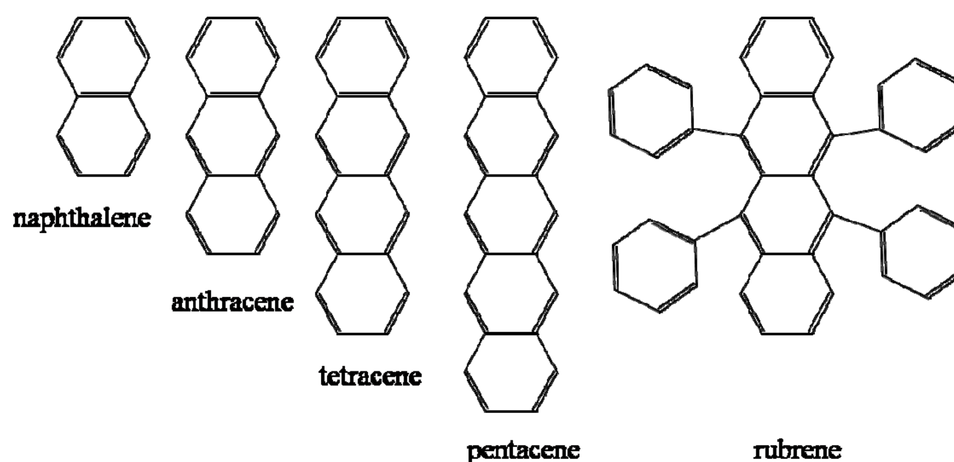

Fig. 1.4: Structure of organic semiconductors based on small molecules.

The linear acene molecules are made up of fused benzene rings (Fig. 1.4). These molecules easily form relatively high quality semiconducting crystals. The acene molecules have sp^2 hybridized carbons in which carbon is bonded to its neighbors by σ bonds. $2s$, $2p_x$ and $2p_y$ orbitals of a carbon atom are hybridized and form the three σ bonds. The remaining $2p_z$ orbital contributes to the formation of a π bond. The delocalization of electrons occurs through the overlap between π orbitals along the molecular chains within a molecule. The organic semiconductors listed in Fig. 1.4 have a conjugated π-electron system where π orbitals of carbon atoms are held together by π bonding.

1.3.2.1 Pentacene

The pentacene molecule consists of five benzene rings. Pentacene forms bulk crystals with herringbone structure in which the face of one molecule is close to the edge of another. Figure 1.6 shows the structure of a layer within a bulk pentacene crystal. The bulk solid consists of a stack of these layers. Pentacene has a crystallized structure with a triclinic lattice structure with a=7.90 Å, b=6.06 Å and c=16.01 Å [51, 52]. Two non-equivalent molecules comprise the unit cell and the longitudinal axes of them have different orientations with respect to the surface normal. The longitudinal axes of two molecules are tilted by 22.1° and 20.3° with respect to the surface normal [52]. At least four different polymorphic structures of pentacene with different intermolecular spacings have been reported [53]. The intermolecular spacings of pentacene layers are determined by substrate temperature during deposition, deposition rate, and thickness of the layer. In this thesis, we studied how the deposition rate can affect the orientation of pentacene molecules on SiO_2.

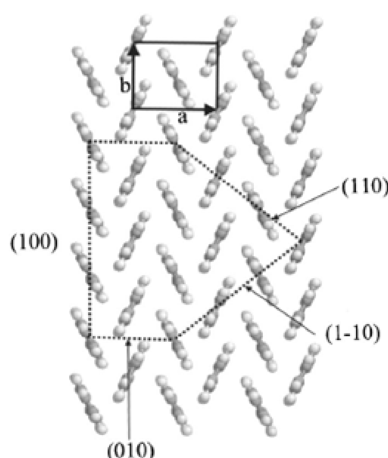

Fig. 1.6: A schematic diagram of one plane of a pentacene crystal [51].

1.3.2.2 Rubrene

Rubrene ($C_{42}H_{28}$) is a benchmark material for organic single-crystal FETs because the field-effect mobility of carriers in rubrene single crystals is the highest reported for organic semiconductors [54, 55]. Rubrene has four phenyl side groups connected to a tetracene backbone. As with pentacene, rubrene can be crystallized in herringbone arrangement with a variety of crystal structures with monoclinic, triclinic and orthorhombic symmetry, depending on the conditions under which the crystals are grown [56-58].

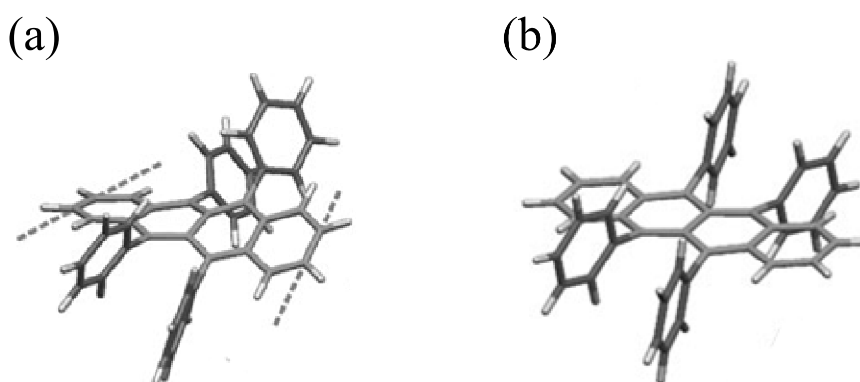

Fig. 1.7: Geometry of a rubrene molecule (a) in the gas phase (b) and in the crystalline phase [56].

Rubrene thin films have been studied because of the ease of process and its potential high mobility. Rubrene has different molecular conformations in gas phase and crystalline phase [56]. The conformation of rubrene deposited on SiO_2 substrate is close to the gas phase. In the gas phase, the tetracene backbone of rubrene is twisted as shown in Fig. 1.7(a). The backbone of the bulk crystalline phase is planar (Fig. 1.7(b)). The molecular energy difference between the two rubrene geometries is about 210 meV [56]. A free

rubrene molecule in the gas phase is more stable. Certain energy is thus needed for free molecules on a substrate to condense from gas phase to the bulk crystalline phase. The energy for the planarized tetracene backbone in the crystalline phase leads to a more ordered packing of rubrene molecules in the bulk. In this thesis, the electrical properties of amorphous rubrene films grown on room temperature SiO_2 have been studied using OFETs.

1.3.2.3 C_{60}

C_{60} has been widely used in OFETs and organic solar cells due to the high mobility of electrons in solid C_{60}. Isolated C_{60} molecules are strong electron acceptors due to their high electron affinity [40]. The 60 carbon atoms in C_{60} form 12 pentagons and 20 hexagons where each pentagon is surrounded by 5 hexagons. The diameter of a C_{60} molecule is 7.1 Å and each carbon atom is bonded to three other carbon atoms via sp^2 hybridized orbitals [60, 61]. The fourth electron in each carbon atom forms π orbital above and below the pentagon and hexagon ring [60, 61].

Thermally evaporated C_{60} molecules crystallize in a face-centered cubic (FCC) structure. The high crystallinity of these films leads to high mobilities up to 1.5 cm^2/Vs in FETs fabricated using C_{60} films. These mobilities are the highest reported among n-type organic semiconductors [37, 62-65]. The high mobility of C_{60} has motivated the use of C_{60} derivatives such as [6, 6]-phenyl-C_{61}-butyric methyl ester (PCBM) which is solution processable, as organic active layers in OFETs [16, 66].

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Chapter 2

Channel Formation in Single-monolayer Pentacene Thin Film Transistors

2.1 Introduction

Electrical properties of organic electronic devices such as OFETs and OLEDs are determined by two important processes, charge injection between metallic electrodes and the organic semiconductors and transport through the organic semiconductors [1, 2]. Therefore, studies of organic semiconductors and the interfaces the organic semiconductors create in the devices are central to device applications.

OFETs are powerful tools for these studies [3]. Charge carriers induced in the organic active layer of OFETs by a gate voltage reside in the first few molecular layers near the gate dielectric [4, 5]. This proximity of the charge carriers in the organic semiconductors to the interface between the organic semiconductor and the gate dielectric makes OFETs very sensitive to the interface. The electronic and structural properties of the interface are thus responsible for the electrical properties of the entire semiconducting layer deposited [4-6].

A transistor consisting of a very thin layer of pentacene can provide information on the electrical properties of the accumulation layer. The coverage of pentacene can be measured in monolayers (ML). Here, 1 ML is equivalent 1.5 nm. Using transistors based on approximately one molecular layer, the electrical properties of pentacene at the interface between pentacene and SiO_2 can be assessed using device parameters such as mobility and

threshold voltage.

The structural properties of polycrystalline pentacene layers can be correlated with charge carrier mobility in OFETs [3, 7, 8]. A high degree of structural order in organic semiconductors is required to achieve high field effect mobilities in OFETs. Strong interactions between π orbitals between molecules found in well-ordered organic semiconducting films can provide efficient carrier transport pathways in organic semiconductors. A large number of studies have been focused on devices using thick films of organic semiconductors [9-11]. The effect of the grain boundary on the field effect mobility of carriers in polycrystalline organic films has been extensively studied. In oligothiophene FETs, the mobility of holes increased linearly with grain size, which shows grain boundaries can act as a bottle neck in transporting charges [12].

Thick film devices, however, are not well suited to explore the charge transport layer because the layers above the accumulation layer add to the structural complexity of the pentacene layers without shedding any light on charge transport in devices.

Chwang *et al*. studied electrical properties of single grains of sexithiophene as a function of the total thickness of the semiconductor film [13]. In these devices, the mobility of charge carriers was 10^{-4} cm^2/Vs, which is two orders of magnitude lower than typical thick film devices [14] and the thickness did not influence the mobility. They demonstrated that the sexithiophene FET is contact limited and this results in a large voltage drop at the contact between gold and the sexithiophene film. Dinelli *et al*. showed that the mobility of holes in sexithienyl thin film transistors did not increase with increasing film thickness after the 2nd molecular layer was completed [15]. The saturated mobility was 0.043 cm^2/Vs.

This value was comparable to those of thick sexithienyl films, 0.02-0.03 cm^2/Vs [16]. In Chwang *et al*., the origin of very poor electrical properties of a single grain sexithiophene was thought to be the high schottky barrier at the contacts. The effect of the metal-semiconductor contacts on the current-voltage characteristics of OFETs can be understood relating to transport of carriers in the channel. Although the high mobility saturated at the low coverage could be linked to the thickness of a conducting channel theoretically predicted, a study of how current voltage characteristics of OFETs can reflect charge transport in the conducting channel and the metal-semiconductor contacts is needed to know the origin of the saturation of the mobility.

Here, we probed the source-drain current of OFETs at very low coverages during the formation of the electrical channel between source and drain electrodes. To isolate the effect of metal-semiconductor contacts from the source-drain current we measured the sheet resistance of the electrical channel using four-terminal devices. The source-drain current from two-contact FETs was interpreted based on the electrical properties of the channel.

We have studied how the conducting channel in a single monolayer transistor is formed during the deposition of pentacene molecules. *In situ* electrical measurements of the accumulation layer allowed us to explore roles of geometric contacts between pentacene islands on SiO_2 substrates. Pentacene was deposited onto two-terminal bottom-contact FETs while the current-voltage characteristic curves of the devices were acquired as a function of the coverage of pentacene. The coverage of pentacene was systemically varied and the structural properties of pentacene islands were studied using atomic force

microscopy (AFM).

During the deposition, pentacene islands come into contact and the onset of the current occurs. After the electrical channel formation in pentacene FETs, the current-voltage characteristics in the devices and the AFM images of pentacene were analyzed to study how the geometric changes in the pentacene molecular layers are related to the charge transport in pentacene. The field effect mobility and threshold voltage were measured from the current-voltage characteristic curves to study the charge transport in pentacene monolayers.

In sheet resistance measurements, pentacene was deposited onto devices with four thin metallic contacts patterned at the corners of a square. The sheet resistance of pentacene was measured as a function of gate voltage applied to the gate electrodes. In order to measure the sheet resistance we used the van der Pauw method [17]. The van der Pauw geometry eliminates the problem arsing from a voltage drop at the metal-semiconductor contact in measuring sheet resistance of pentacene layers. These measurements enable us to eliminate the metal-semiconductor contact effects. This approach allows us to measure the mobility of holes of the pentacene molecular layers independent of the contact resistance. The much higher mobilities observed in the sheet resistance measurements of pentacene monolayers using four electrical contacts than from two-terminal FETs indicate that the two-terminal pentacene FETs are contact limited. In the two-terminal FET devices, the contact resistance was calculated from the total resistance and the sheet resistance of the pentacene layer at the coverage of 1 ML. The contact resistance was approximately 10^9 Ω and this value was much larger than the channel resistance of the pentacene layer, $10^6\,\Omega$.

The sheet resistance in the four-terminal devices depended on the pentacene coverage. The small changes in the structure of pentacene layers near the SiO_2 gate dielectric were critical to the charge transport of holes in the pentacene molecular layer.

2.2 Experimental methods

For both two-contact FET devices and four-contact van der Pauw geometry devices, the substrate was a 200 nm thick silicon oxide layer on a highly doped silicon wafer which acts as the gate electrode. The capacitance per unit area of the gate dielectric is 1.7×10^{-8} F/cm^2. We patterned 60 nm-thick Au electrodes on a 10 nm-thick Cr adhesion layer for source and drain electrodes on SiO_2 using photolithography. The channel length and the width were 10 μm and 1 mm, respectively. In the four-contact devices, the electrodes were separated by 2 mm and their width was 500 μm. Pentacene films were grown on the SiO_2 substrate using thermal evaporation under a pressure of 10^{-6} torr or less. The deposition rate was determined by dividing the coverage measured using AFM images of pentacene films by the deposition time. The substrate temperature was kept at room temperature during the pentacene growth and electrical measurements.

In order to study the channel formation in two-contact pentacene FET devices, an electric field was applied between source and drain electrodes and between the gate dielectric and the pentacene layer. The gate voltage was scanned periodically during the deposition, with a fixed source-drain voltage. This continuous gate voltage scan was designed to allow the magnitude of the current flowing through the channel and threshold voltage to be measured as a function of the thickness of the pentacene layer.

In addition to these continuous measurements, the deposition was paused at several coverages and current-voltage characteristics at theses coverages were obtained.

In two-contact FET devices, the transistor parameters were obtained from the electrical measurements by analyzing them using the conventional MOSFET description of the current voltage characteristics [18]. The mobility, μ_{fet}, and threshold voltage, V_T, in the linear and saturation regime was measured based on equation 1.3 and 1.2, respectively. We measured the sheet conductance of pentacene films ranging from 1 ML to 1.6 ML using van der Pauw method. In van der Pauw measurement, a small current at the level of a few nanoamperes was applied using two of the contacts. The voltage difference in the other two contacts was measured. The sheet resistance was calculated based on the eight measurements in which a series of voltage measurements are carried out switching electrodes while current is applied between the other two contacts [17]. For gate voltages higher than the threshold voltage, V_T, the two dimensional carrier density p in the pentacene layer can be expressed by $p= C_{gd} (V_G - V_T)/e$. Here, e is the electronic charge. Since the sheet conductance $\sigma_\square$ is expressed by $\sigma_\square=1/R_s=pe\mu_{eff}$ the mobility, μ_{eff}, of the charge carriers is given by:

$$\mu_{eff} = \frac{\frac{1}{R_s}}{pe} = \frac{1}{C_{gd}} \frac{\partial \frac{1}{R_s}}{\partial V_G} \tag{2.1}$$

Here, R_s represents sheet resistance. The slope of the sheet conductance as a function of V_G can thus be used to find the mobility of holes in the accumulation layer. The most important assumption for the van der Pauw measurement is that all of the charge carriers induced by the gate above threshold voltage are mobile. Here, we use μ_{eff} and μ_{fet} in

representing mobility of pentacene layers. μ_{eff} is the value obtained from van der Pauw sheet resistance measurements based on equation 2.1. This mobility is independent of the contact resistance between metal and organic semiconductors. μ_{fet} is the two-contact FET mobility in the linear regime.

2.3 Percolation of pentacene islands on SiO_2

The geometric arrangement of the pentacene islands is closely related to the conducting behavior of the charge carriers confined in the islands, which is crucial in determining the charge transport in pentacene layers.

Fig. 2.1 shows the drain current as a function of pentacene coverage in a two-contact FET device. The drain current at each coverage was measured at the gate voltage of -100 V and a drain voltage of -50 V. In order to measure the deposition rate, bare SiO_2 substrate was placed next to the FET device during the deposition. After 7 minutes, the bare SiO_2 substrate was blocked from the deposition by a shutter installed in the deposition chamber. The deposition was continued on the FET device to measure current as a function of coverage. The deposition rate was obtained from the coverage of pentacene deposited on the bare SiO_2 substrate and the deposition time. The coverage of pentacene checked by the AFM image of the pentacene film on the bare SiO_2 substrate was 1.2 ML and the deposition rate was 0.17 ML/min. In calculating the coverage, we assumed that molecules are packed and arranged in the same way in each molecular layer. For pentacene coverages below 0.77 ML, a drain current less than 20 pA was observed. This was the leakage current through the gate dielectric before depositing pentacene.

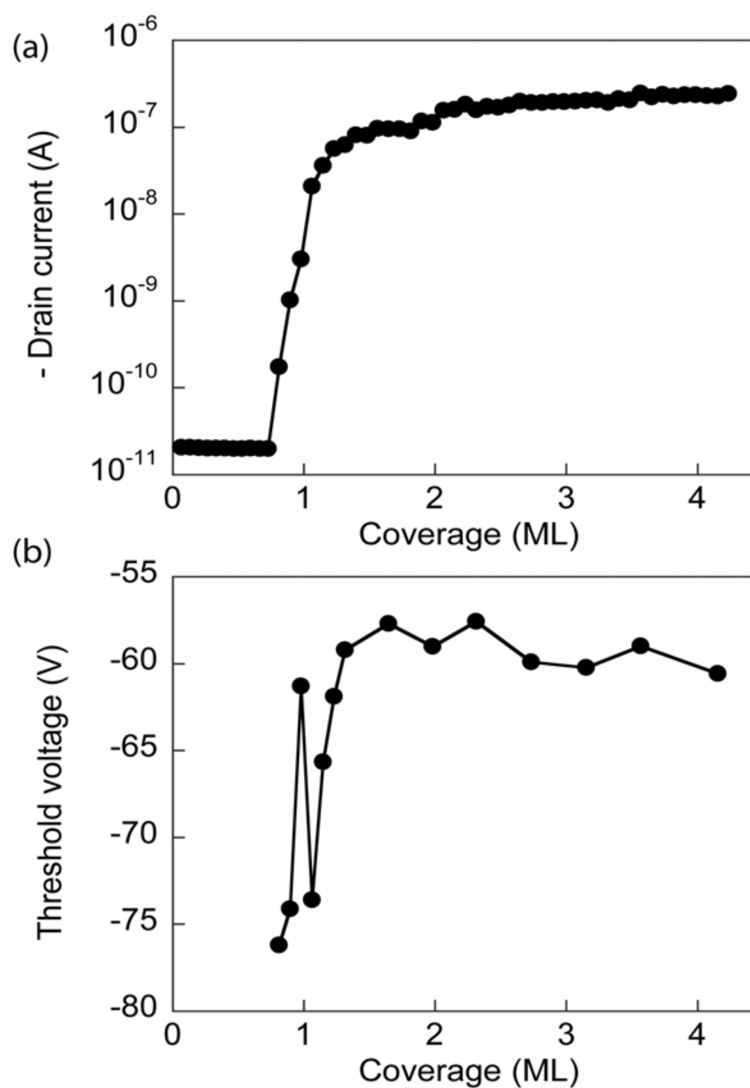

Fig. 2.1: (a) Drain current and (b) threshold voltage as a function of pentacene coverage during the formation of a bottom-contact pentacene FET. The current in (a) is measured at V_G= -100 V during a series of gate voltage scans from -70 V to -100 V with a source-drain voltage of -50 V.

Current began to flow through the channel at a coverage of 0.77 ML. The drain current increased rapidly with the coverage of pentacene as the coverage increases from 0.77 ML

to 1.2 ML. After the coverage exceeded 1 ML, the drain current was not sensitive to the coverage of pentacene.

The onset of current at a particular coverage observed in current vs. coverage plots can be explained by the geometric percolation of pentacene islands. The steep slope in the plot after the percolation threshold supports the geometrical change between islands. At the percolation threshold a current path has been formed by a geometric connection of pentacene islands. In a continuous two-dimensional system, the percolation threshold of a pentacene transistor is expected to occur when the area occupied by pentacene islands reaches 67% of the total channel area in the device [19]. This threshold value varies only slightly with changes in the distribution of island sizes and deviations in shape away from circular islands [20]. In terms of the electronic properties of the transistor, the current path between the source and drain is formed at the percolation threshold. Similar phenomena have been observed in the growth of metal clusters on SiO_2 and in the formation of rubrene thin film transistors [21, 22]. In both of these cases, however, the formation of three dimensional islands at low coverages complicates the geometric description of the percolation transition.

In a number of *in situ* experiments, the coverage at which current began to flow was distributed between 0.69 ML and 1.3 ML. We suggest that this phenomemnon is due to the high threshold voltage of the devices. Threshold voltage has been linked to the trap density [23, 24]. According to Podzorov *et al.*, below the threshold voltage, charges injected from metal electrodes are trapped in the localized states which are located more than a few k_BT above the highest occupied molecular orbital (HOMO) level. The trapping states are

believed to result from impurities and structural disorders introduced during growth of organic semiconductors [24]. Above the threshold voltage, the charges fill the trap sites. A high threshold voltage is thus related to a high trap density [23, 24]. The trap density can be expressed by [24]:

$$N_{trap} = \frac{C_{gd} V_T}{e} \qquad (2.\ 2)$$

Here, N_{trap} represents the concentration of traps.

We suspect that the traps are not uniformly distributed. When islands finally touch each other, the contacts could produce a higher trap density at the junction due to the misorientation between islands, and a higher threshold voltage at the contact can be expected.

The current onset after 1 ML at our percolation threshold measurements is thought to be due to the delay caused by a very high threshold voltage at the junction. Although the coverage of pentacene on SiO_2 exceeded the theoretically predicted percolation threshold, 0.67, a high structural disorder at the contact between islands induces a high trap density and this prevents mobile charge carriers from accumulating at the junction, resulting in a high contact resistance at the junction. The threshold voltage for the device is thus not attainable in the scan range of the gate voltage in our percolation experiments.

The threshold voltage below 1 ML in Fig. 2.1(b) was close to 80 V. This is much higher value compared with those of thick pentacene FETs. The threshold voltages of thick pentacene films are in the range between -30 and 30 V. The trap density of 1 ML pentacene is 9×10^{12} cm^{-2} based on equation (2.2). The molecular density of the single crystal pentacene is 2.9×10^{21} cm^{-3} [25] and the thickness of 1 ML pentacene is 1.5 nm. From the

trap density and the two dimensional molecular density of pentacene, 2 trap sites per 100 pentacene molecules were found.

The threshold voltage decreased rapidly after the percolation threshold (Fig. 2.1(b)). After the formation of a two dimensional channel, the threshold voltage no longer decreased with a further increase in the pentacene coverage. Judging from the saturation of the threshold voltage after 1 ML, the coalescence between pentacene islands has a crucial role in determining the threshold voltage. We suggest that the saturation of the threshold voltage is related to the finite trap density. Coalescence between pentacene islands reduces the number of trap sites and the threshold voltage decreases. If this is the case, once the first layer is completed, the structural disorder at the junction no longer decreases and the threshold voltage should remain constant.

2.4 Electrical and structural properties of monolayer pentacene on SiO_2

The structural changes of pentacene islands on SiO_2 in the FET have large effects on the electrical properties of the pentacene layers. The roles of the geometrical connection between pentacene islands and the formation of the interface between pentacene and SiO_2 in determining the magnitude of the source-drain current are clearly illustrated in Fig. 2.2 and Fig. 2.3. Fig. 2.2 shows AFM images of systematically varied pentacene thickness on oxidized silicon from 0.3 ML to 1.24 ML. Between 0.3 ML (Fig. 2.2 (a)) and 0.6 ML (Fig. 2.2 (b)), the size of the islands size increases laterally.

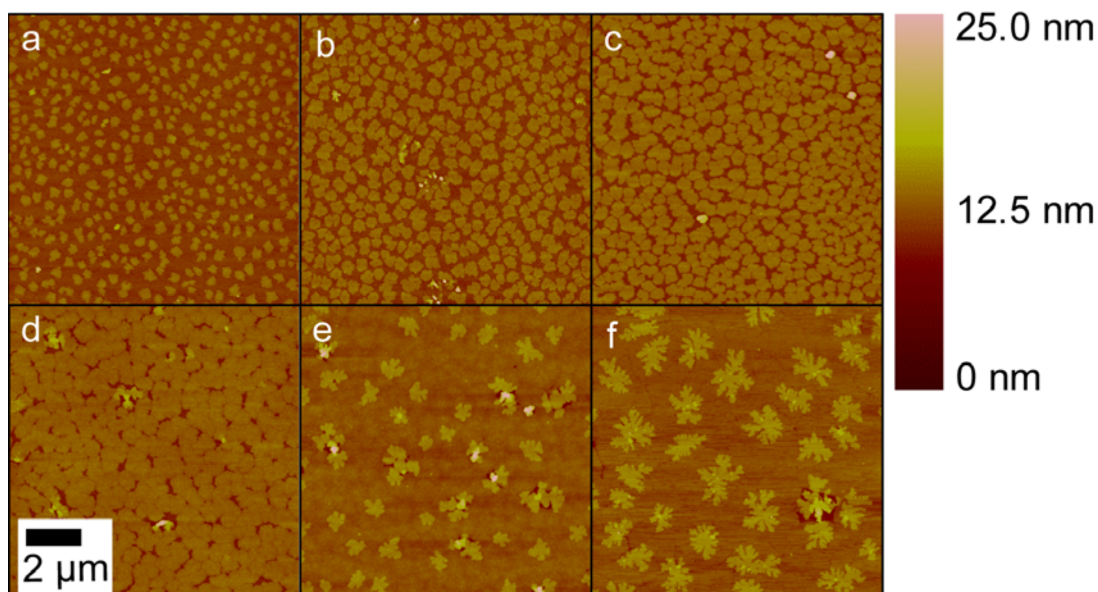

Fig. 2.2: Atomic force microscope images of pentacene island formation on SiO_2 substrates at pentacene coverages of (a) 0.30 ML, (b) 0.60 ML, (c) 0.75 ML, (d) 0.92 ML, (e) 1.15 ML, and (f) 1.24 ML.

The heights of the islands are 1.58±0.06 nm. These heights are measured using line scans from the AFM images. This value is comparable to the interplanar spacing of pentacene molecules grown on SiO_2, where pentacene molecules are slightly inclined with respect to the normal of the substrate. In XRD experiments interplanar spacing of the single crystal pentacene was 14.5 Å. For pentacene films deposited in vacuum the height was 15.4 Å [26-28].

The charge transport in the submonolayer regime was studied by analyzing the current-voltage characteristic curves at two submonolayer coverages (0.72 ML, 0.9 ML), during pauses in the deposition. The results of the electrical measurements are shown in Fig. 2.3. Figure 2.3(a) shows the drain current as a function of pentacene coverage during this

experiment. The drain current at each coverage is plotted for the point in the gate voltage scan at which V_G=-80 V. The measurements were made at a fixed drain voltage of -50 V. Output characteristic curves are shown in Fig. 2.3 (b) and (c) at coverages of 0.72 ML and 0.9 ML, respectively. In these scans a more negative gate voltage caused a higher drain current at the same drain voltage as seen in typical *p*-type FET.

The AFM images at 0.72 ML and 0.9 ML in the inset of Fig. 2.3(a) shows the arrangement of pentacene islands in the sample, for which the electrical measurements are shown. The increased current at the higher coverages is due to the coalescence between islands. The islands are better connected to each other at 0.9 ML than at 0.78 ML. At the higher coverages the number of the contacts between islands and the contact area between islands was increased. These made the submonolayer transistors more sensitive to the change in the coverage of pentacene than to the contacts between pentacene layers and metal electrodes. The mobility measured using the two-contact FET device (Fig. 2.3(c)) for 0.9 ML was 9.8×10^{-4} cm^2/Vs.

In Fig. 2.2(e), at a coverage of a 1.15 ML, a nearly completed, first pentacene layer coexists with islands in the second layer of molecules. The shapes of the islands in the second layer in Fig. 2.2(e) and (f) are dendritic, which is different from the circular shapes of the islands in the first layer. Islands in the third and higher layers of molecules were observed in Fig. 2.2(e). The formation of islands in the higher layers indicates that the kinetic processes governing pentacene island growth are quite different when pentacene molecules are grown on top of pentacene islands compared with pentacene islands on SiO_2. The Ehrlich-Schwoebel barrier for molecules descending from the first layer to the SiO_2 is

significantly lower than descending from the second to the first pentacene layers [29, 30]. Because the third layer islands nucleate almost immediately, the second layer of islands does not percolate as easily as the first monolayer.

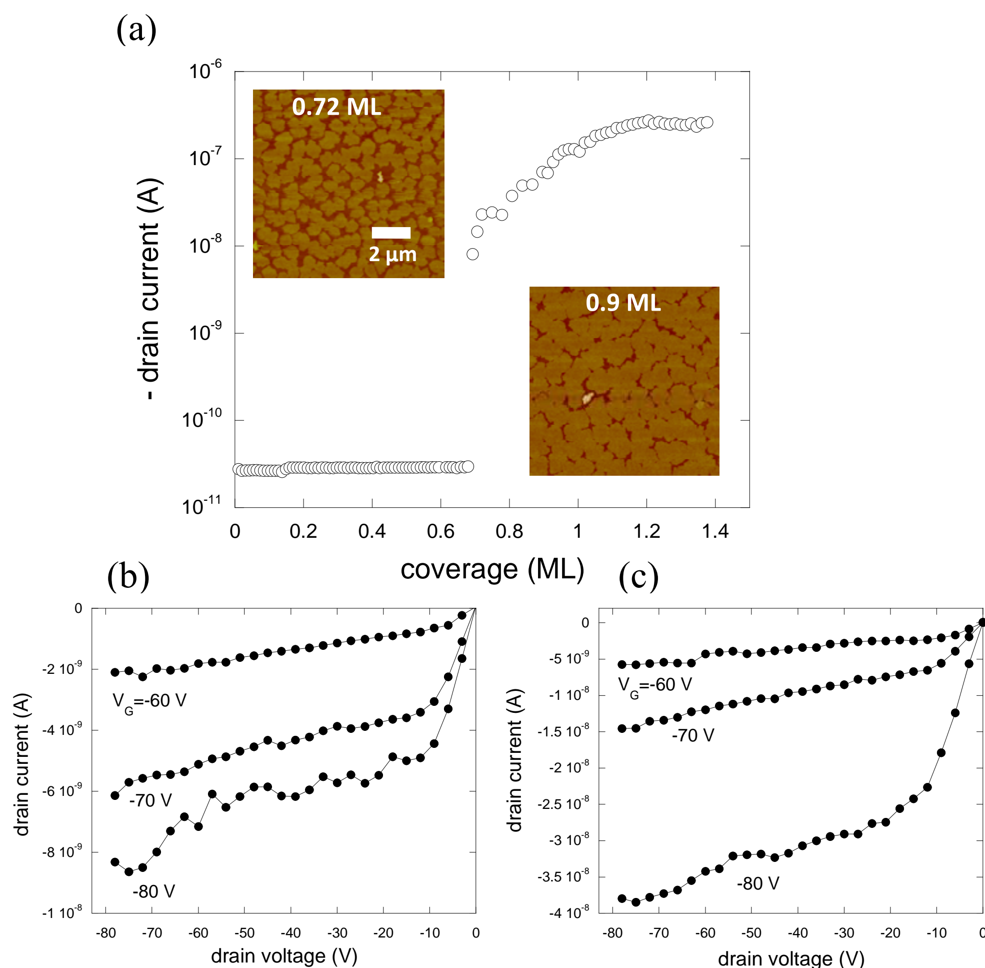

Fig. 2.3: (a) Drain current as a function of pentacene coverage. The drain current at each coverage was measured at a constant gate voltage (-80 V) and drain voltage (-50 V). The inset shows AFM images at 0.72 ML and 0.9 ML. (b), (c) Transistor characteristic curves at 0.72 ML and 0.9 ML.

Increasing the pentacene coverage also led to higher charge carrier mobilities in our in situ electrical measurements. The FET mobility, μ_{fet}=9.8×10^{-4} cm^2/Vs in the submonolayer transistor, was still much lower than that of typical thick pentacene films (Fig. 2.3(c)). This is surprising because most charge transport in FETs occurs in the first few layers close to gate dielectric. Most of the induced charges by the gate voltage reside in monolayer pentacene and the mobility measured at 0.9 ML is expected to be close to those of thick pentacene FETs.

One possible explanation for the low mobility is that the barriers to carrier injection at interfaces with the source and drain electrodes can change the magnitude of drain current by lowering the voltage drop across the channel. The barriers in thicker films have been investigated using scanning Kelvin probe microscopy and four probe method [31-33]. In those studies, a significant fraction of the total voltage between the source and drain appears across the metal-semiconductor contacts. Interpreting this electrical phenomenon microscopically is challenging because the area of the contact between single-molecule-high pentacene islands and the metal electrodes can be structurally different from the bulk.

2.5 Contact resistance in monolayer transistors

The transport of holes in pentacene can be precisely probed in a monolayer of pentacene using devices in which the effects of the contact resistance is eliminated. In order to measure the electrical properties of a monolayer without contact resistance effects, we used the van der Pauw method [17]. For the measurement, pentacene was deposited onto a device where four gold contacts were formed lithographically. For the samples, a current of several nA produced voltages of less than 1.5 V at all contacts. These low voltages indicate

that the pentacene film was biased into the linear rather than saturation regime. A gate voltage larger than a threshold voltage leads to the accumulation of holes.

Fig. 2.4(a) shows the dependence of the sheet conductance obtained from van der Pauw measurements on gate voltage, V_G. In this experiment, pentacene was deposited on the four-terminal devices and the electrical measurements were carried out in the deposition chamber. The mobility obtained from the slope of sheet conductance as a function of V_G using equation 2.1 was 0.085 cm^2/Vs. Surprisingly, the effective mobility (μ_{eff}) is approximately two orders of magnitude larger than the mobility (μ_{fet}) value determined from two contact FETs.

The large contact resistance in pentacene monolayer FETs suggests that there are two regimes in which different phenomena limit the mobilities of charge carriers. The first regime is one in which charge injection at the contacts is the dominant effect. In a second regime, the geometric change in pentacene islands dominates the charge transport in pentacene. For submonolayer coverages just above the percolation threshold and up to 1.2 ML, the contact between islands is responsible for changes in the current and threshold voltage.

At higher coverages, after completing the first molecular layer, the resistance between the pentacene layer and the contacts becomes important. At these higher coverages, the two terminal devices operate in a contact limited regime. In Fig. 2.3(a), the source-drain current of the two terminal device was saturated after 1.2 ML and the mobility, μ_{fet} was very low (~10^{-3} cm^2/Vs). This indicates that at the higher coverages the two terminal devices reflect changes in the contacts rather than in the electrical properties of the pentacene layer [32].

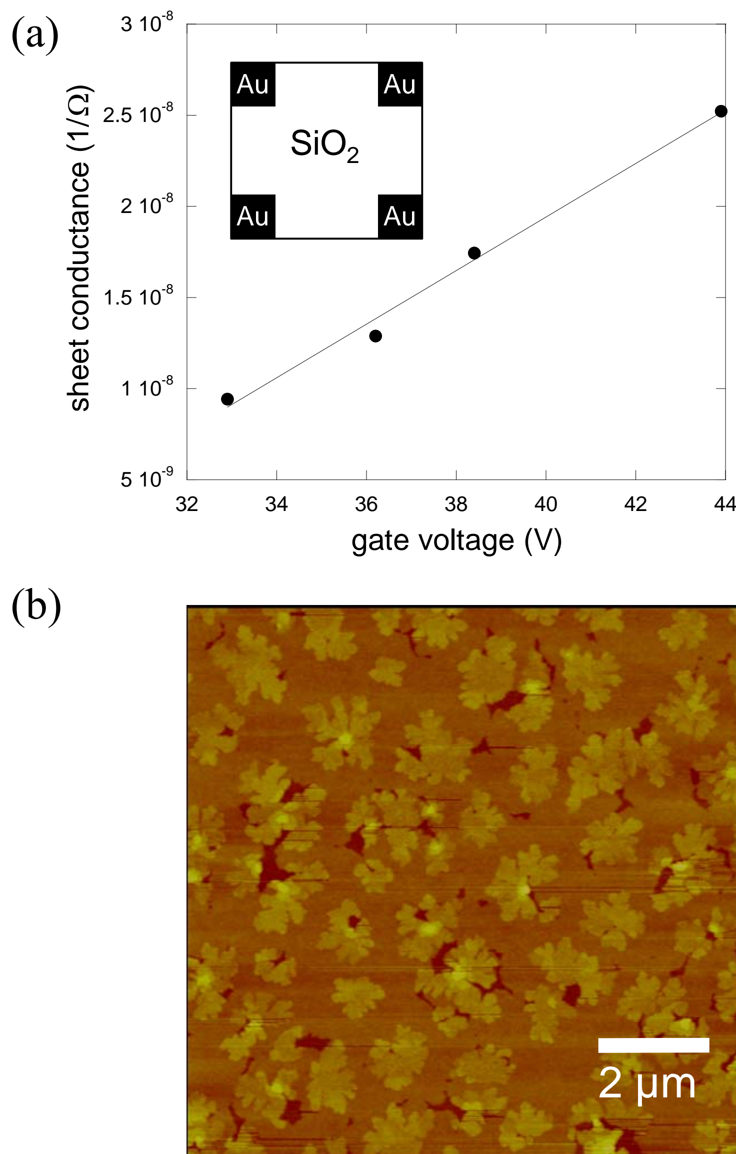

Fig. 2.4: (a) Sheet conductance (1/Ω) as a function of gate voltage for a 1.4 ML thick pentacene film. The inset shows a schematic of the van der Pauw geometry device. The four black squares are the gold electrodes. (b) AFM image of the sample used to obtain the electrical results in (a).

Charge transport in the accumulation layer close to the SiO_2 surface can be systemically studied by measuring the mobility as a function of the pentacene coverage. The source-drain current in the contact limited device of two contact FET didn't reflect the change in pentacene islands after 1 ML during growth. Using four-terminal devices, we studied how structural changes in pentacene islands can contribute to the transport of holes in pentacene films around 1 ML. We deposited pentacene onto three van der Pauw geometry devices with different thickness. After deposition we removed these samples from the vacuum chamber and, after wiring them in air, measured the sheet resistance as a function of gate voltage under vacuum in the deposition chamber. The probe current for the sheet conductance measurements in Fig. 2.5 was 4.2 nA.

Fig. 2.5 (b) shows the AFM images of pentacene at the coverage ranging from 0.99 ML to 1.6 ML. At the coverage of 0.99 ML pentacene islands on SiO_2 are bright and the SiO_2 substrate dark. At this coverage, vacant sites between pentacene islands are still being filled by additional pentacene and second-layer islands are visible on top of the first layer. The mobility of holes in the 0.99 ML pentacene layer was 0.016 cm^2/Vs.

At higher coverages, as more pentacene molecules were added, the vacant sites between islands were almost completely filled and second layer islands grew laterally. At the coverage of 1.32 ML the dark-colored substrate is rarely seen and islands with dendritic shapes on the completed layer are observed. At the coverage of 1.6 ML the first layer was completed. For a 1.32 ML film, the mobility was a factor of two higher than at the lower coverage even though the pentacene coverage had only increased by 30%. With 1.6 ML the second layer islands were larger, with the beginnings of the third layer on top of them (Fig.

2.5(b)). The change in mobility across the range of coverages on these three samples was striking, with μ_{eff} increasing from 0.016 cm^2/Vs with 0.99 ML to 0.15 cm^2/Vs at 1.6 ML.

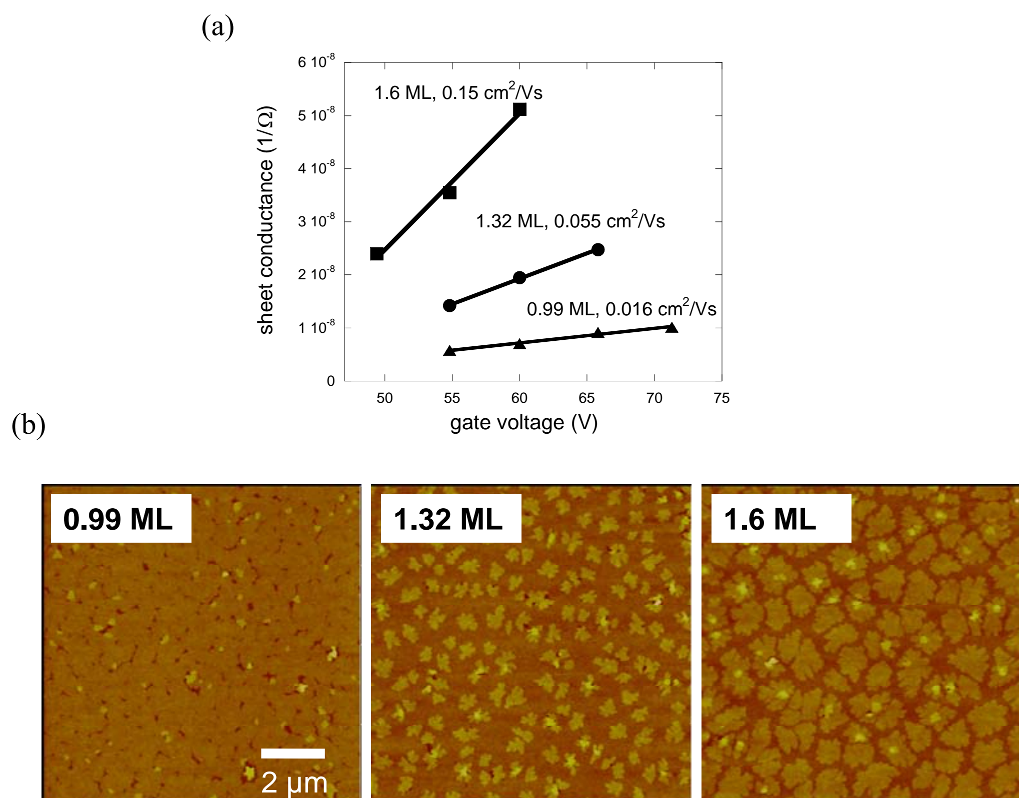

Fig. 2.5: (a) The sheet conductance of pentacene films at three different pentacene coverages (0.99 ML, 1.32 ML and 1.6 ML) as a function of gate voltage. The current for these sheet conductance measurements was 4.2 nA. AFM images for each device are shown in part (b).

The differences between the measurements with two-contact FETs and the four-contact van der Pauw geometry structures can be used to estimate the resistance at the contacts

between the metal electrodes and the pentacene monolayers. The large difference between the mobilities observed with two and four terminals shows that the vast majority of the total resistance was assigned to the contact resistance between metal and pentacene.

Even though the second layer islands did not come into contact, the sheet conductance and mobility increased with increased coverage. The second layer islands can contribute to electrical charge transport by adding a parallel conduction path and locally reducing the resistance of areas covered by a second layer island. The improvement in the two-terminal mobility μ_{fet} observed in two-terminal devices could be caused by either the large improvement in the channel mobility or, more likely, by improvements in the physically incomplete contact between the metal and the pentacene.

2.6 Conclusions

We have found that pentacene monolayer transistors are sensitive probes of the charge transport in pentacene. Molecular layers of organic semiconductor can be incorporated into numerous applications such as OLEDs and organic solar cells. The transport of carriers in the layers can affect the performance of the device. Our system can be applied to study the electrical properties of other organic semiconductor materials that could potentially be used as a charge transport layer in the devices. The effects of crystal structure and morphology of organic semiconductors at low coverages grown under different deposition conditions on charge transport in organic semiconductors can be explored more precisely.

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Chapter 3

Orientation of Pentacene Molecules on SiO_2 :

From a Monolayer to the Bulk

3.1 Introduction

As shown in our studies of the formation of the channel in pentacene monolayer transistors in Chapter 2, the interface between pentacene and SiO_2 is very important in determining electrical properties of devices. Subtle changes in pentacene molecular layers close to SiO_2 led to dramatic changes in the conductivity of the pentacene layers. A study of the structural properties of the pentacene layers at low pentacene coverages is thus essential in understanding the interface.

Fritz *et al*. measured the in-plane lattice parameters of a monolayer thick pentacene film on SiO_2 using grazing angle incidence x-ray diffraction (GIXD) [1]. They found that the lattice parameters are different from those of thicker pentacene films. Furthermore, they observed that, at submonolayer coverages, pentacene molecules stand up and the longitudinal axis of the pentacene molecule is oriented at a smaller angle with respect to the surface normal than that of a molecule in bulk pentacene. Other studies have found that pentacene thin films on SiO_2 can form two different phases of a thin film and bulk phase with different lattice constants and molecular orientations [2]. In both phases, pentacene molecules stand nearly upright with different interlayer spacings [2]. This difference indicates that the pentacene molecules are oriented with different angles respect to the

surface normal in the two phases.

X-ray diffraction studies have found that the thin film phase and the bulk phase coexist in thin films on an oxidized silicon substrate [3]. In the diffraction experiments, no critical thickness separated the thin film phase and the bulk phase.

We have attempted to address this problem by probing the molecular orientation of pentacene thin films with thickness ranging from below 1 ML to 90 nm. Our goal was to understand how the molecular orientation changes depending on the deposition conditions. We collaborated with Fan Zheng of Prof. Franz Himpsel's group. Near edge x-ray absorption fine structure spectroscopy (NEXAFS) has previously been used to study the orientation of planar aromatic molecules [4, 5]. It is complementary to x-ray diffraction (XRD) study in probing the structural properties of the pentacene film. The probing depth of NEXAFS is 10 nm and this enables NEXAFS to probe the orientation of the molecules in low pentacene coverages. NEXAFS complements XRD in this sense because XRD probes the molecular layer spacing and typically requires thicker films on the order of 20 nm [2].

3.2 Experimental methods

The physical basis for NEXAFS is that x-ray photons absorbed in a molecule can excite electrons from a core level (C 1s) to empty anti-bonding orbitals (π^* and σ^*). Auger and secondary electrons leaving the sample provide a signal proportional to the primary absorption events. As the number of absorption events increases, the number of electrons detected increases. The total electron yield (TEY) was acquired by counting electrons emitted from the sample surface. The molecular orientations of pentacene were calculated

from the TEY results. The absorption spectra were normalized to the incident photon flux via the photocurrent of a clean gold sample.

A silicon wafer with a thermally grown 200-nm-thick silicon oxide layer was used as the substrate for the pentacene thin films. The substrate was cleaned with acetone and methanol in an ultrasonic bath and rinsed with deionized water in a clean room. Pentacene in an effusion cell was thermally evaporated in a vacuum chamber with a working pressure of 2×10^{-6} torr without any prior purification. During the deposition the substrate was kept at room temperature.

3.3 Polarization-dependent NEXAFS and molecular orientation

NEXAFS data can be analyzed using structural models for the orientation of pentacene molecules on the SiO_2 substrate. The angle α corresponds to the angle between the surface normal and the π^* orbitals, which are perpendicular to the plane of the rings within pentacene molecule (Fig. 3.1). We have deduced this angle for pentacene films grown at different deposition rates and film thicknesses. A separate angle, γ is the angle between the longitudinal axis of the pentacene molecules and the substrate.

Fig. 3.2 shows an example of a C 1s NEXAFS spectrum. There are several absorption features arising from resonant absorption at π^* and σ^* transitions. The peaks between 283 eV and 288 eV arise from excitations of C 1s electrons into π^* orbitals. This π^* transition region consists of at least twelve components. The broadened peaks at higher energies are due to σ^* transitions. The π^* transitions have two pronounced peaks, 1 and 2, which correspond to transitions into the lowest unoccupied molecular orbital (LUMO) and the

next higher orbital. Each peak can be assigned to specific C atoms, as shown in the inset of Fig. 3.2 [7].

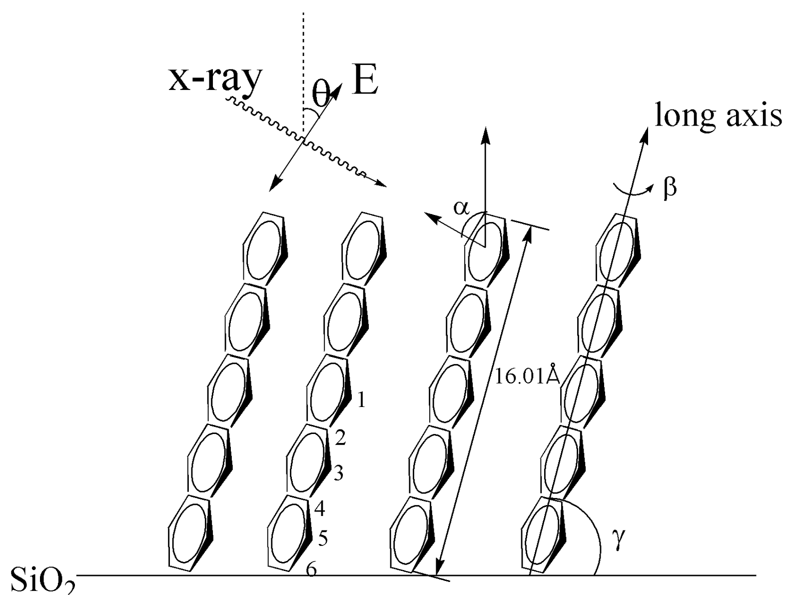

Fig. 3.1: The geometry of thin pentacene films. The pentacene molecule can be rotated around its long axis by an angle β, the angle α is not necessarily equal to γ. θ is the angle of the electric field vector of the incident soft x-ray radiation measured from the surface normal.

The inset of Fig. 3.2 displays the contributions of the 6 nonequivalent carbon atoms to the π* transitions. The first pronounced peak in the π* consists of the contributions from transitions at carbon atoms 1, 3, 5, and 6 while transitions at carbon atoms 2 and 4 are related to the second pronounced peak in the π* region [7]. The length of vertical bars assigned to 6 atoms represents the degree of contributions to the π* transitions.

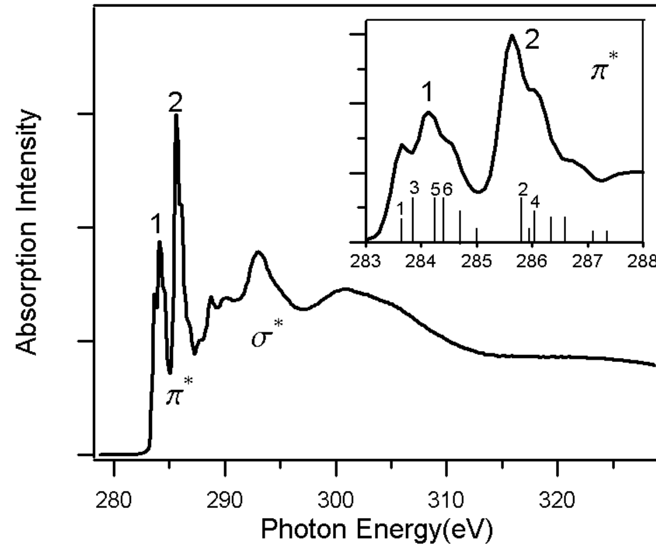

Fig. 3.2: The NEXAFS spectrum from a pentacene deposited at a rate of 0.1 ML/min to a total film thickness of 90 nm on SiO_2. The inset shows the π^* region together with the peak assignments for the dominant π^* transition based on ref. 7.

The absorption cross section depends on the orientation of the electric field vector of the photon with respect to the direction of transition dipole moment [5, 8]. When the electric field vector of the the incoming x-rays is perpendicular to the ring planes, the absorption due to the π^* resonance intensity is a minimum. The absorption has a maximum intensity when the electric field vector is aligned parallel to the ring planes of the pentacene molecules [5]. With linearly polarized photons, well oriented films produce spectra that depend on the incident angle of photon [5, 9].

The tilting angle α can be calculated using the equation below:

$$\frac{I_v(\theta)}{I_v(\theta=90)} = 1 + P \times (\frac{2}{\sin^2 \alpha} - 3) \times \cos^2 \theta \qquad (3.1)$$

Here, θ is the photon incidence angle and I_v is the measured absorption intensity as a function of the angle θ. In analyzing the data, the spectra are normalized to the intensity at a 90˚ angle of incidence. A series of intensity measurements at different incident angles, θ, are used to measure the tilting angle α using equation 3.1.

In extracting the tilting angle, we have assumed that the pentacene molecules are uniformly distributed azimuthally over the deposited area. Also we have to take into account that there are two non-equivalent pentacene molecules comprise in each unit cell of the pentacene crystal [10]. The longitudinal axis of a pentacene molecule is tilted with respect to the surface normal and the tilting angles of two non equivalent molecules within the unit cell are each different. According to the crystallographic data on bulk pentacene, the tilting angle α of two non equivalent molecules differs by 13.1° [10].

3.4 Molecular orientation of pentacene on SiO_2

3.4.1 Effect of thickness on molecular orientation

The comparison of the angle α between films with submonolayer thicknesses and thick films can provide information on the dependence of the molecular orientation on the thickness of pentacene thin films.

Fig. 3.3 shows NEXAFS spectra for several angles of incidence of the photon beam ranging from 20° to 90°. These spectra were acquired for both submonolayer and 90 nm thick pentacene films grown at the same deposition rate. In Fig. 3.3, the π^* transitions decrease in intensity as the incidence angle decreases and the σ^* transitions evolve in the opposite way.

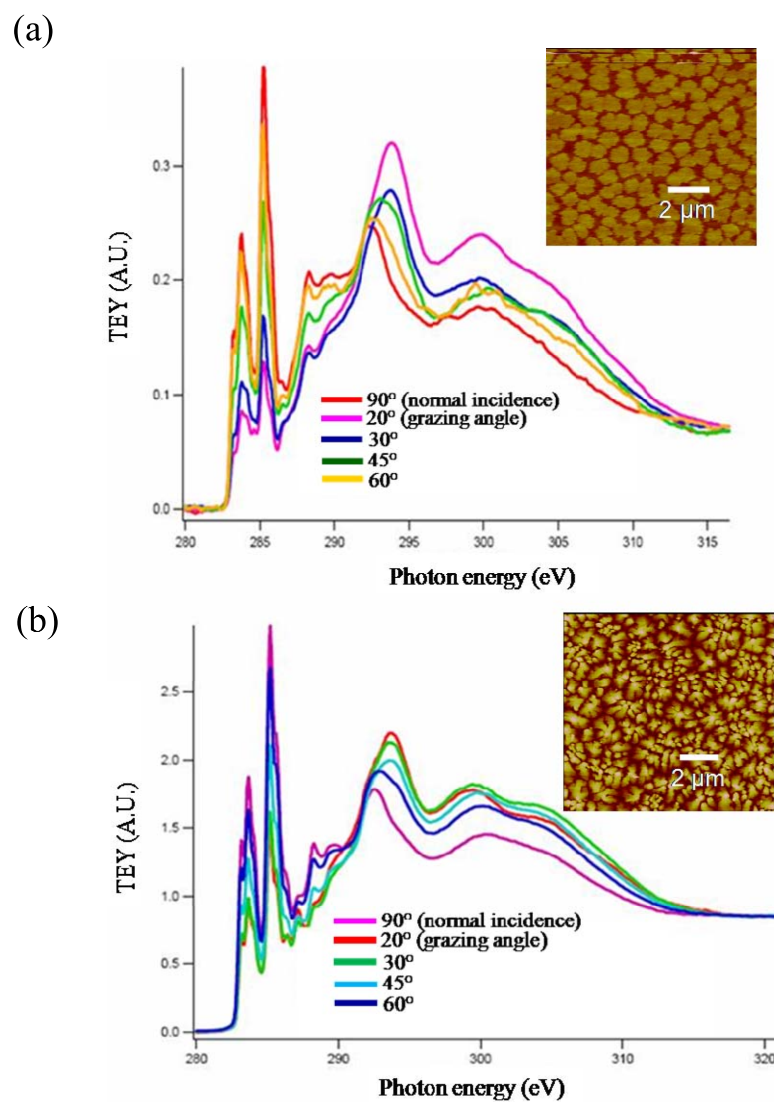

Fig. 3.3: The NEXAFS spectra and AFM images of (a) 0.7 ML and (b) 90 nm pentacene films.

The angular dependence of the intensity of the resonant absorption at the π* transition indicates that the submonolayer and the thick pentacene films are molecularly well oriented on SiO_2. If the longitudinal molecular axis of pentacene, however, were in the

plane of the surface we would observe the same angular dependence in the absorption spectra. Our AFM images in the insets of Fig. 3.3 rule out this possibility. The values of α deduced from the data in Fig. 3.4(a) and (b) are 72° and 66°, respectively.

3.4.2 Effect of deposition rate on molecular orientation

We have repeated this analysis for spectra acquired from films grown under a range of deposition conditions. Fig. 3.4 and 3.5 shows that different deposition rates produce thin films with different values of the orientation angle α. The coverages for these two samples are 1.4 ML for Fig. 3.4(a) and 1.1 ML for Fig. 3.4(b), respectively. Fig. 3.4(a) and (b) show AFM images of the pentacene thin films grown at high and low deposition rates, respectively. In Fig. 3.4(a), the first layer has been completed and the second layer islands have dendritic shapes. At the low deposition rate sample, Fig. 3.4(b), the 1st layer has not been completed and 2nd islands are already visible. The angle α for high and low deposition rates are 74° and 67°, respectively.

We systemically varied the deposition rate and deposited films with a number of coverages. Fig. 3.5 shows the molecular orientation α for films grown at three different deposition rates ranging from 0.008 ML/min. to 1.5 ML/min. The angle α does not change significantly as a function of coverage within each grouping, such that we can take the average angle $\langle\alpha\rangle$ for each grouping as representative of the entire group. This average is shown as the horizontal lines in Fig. 3.5. The pentacene layer grown with a low deposition rate has the smallest angle α.

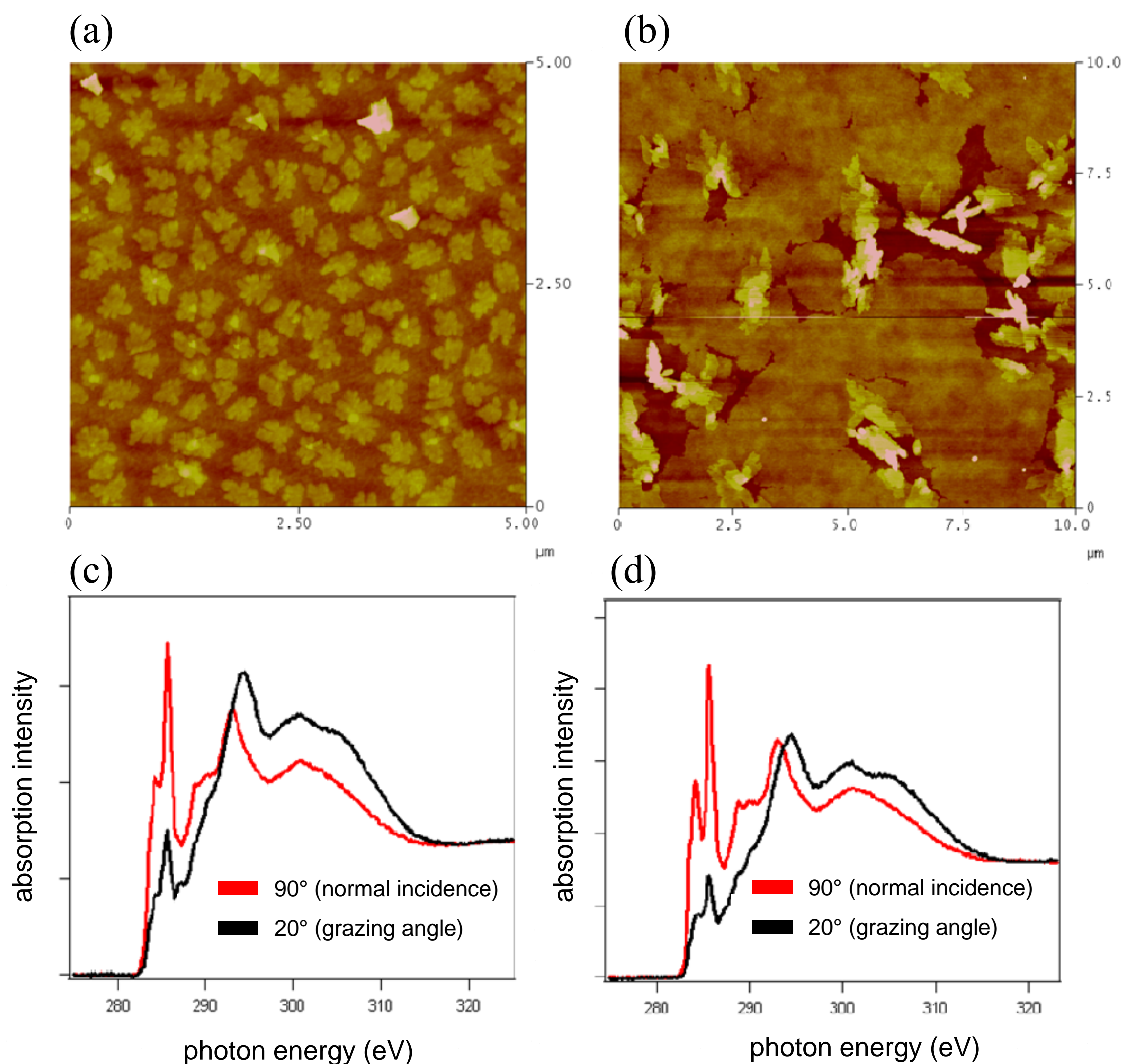

Fig. 3.4: AFM images and NEXAFS spectra of pentacene films grown at deposition rates of 1.5 ML/min for (a) and (c), and 0.008 ML/min for (b) and (d).

The dependence of the molecular orientation on the deposition rate can be explained in two different ways. One explanation is that each particular deposition rate produces a structurally distinct crystalline phase on the substrate and a number of phases can exist separately depending on the deposition rate. The long axis of pentacene molecules

deposited at a low deposition rate has a larger angle with respect to the surface normal than those formed at the higher deposition rate. This trend is found in Fig. 3.5. The average angle <α> for the deposition rates for 0.008 ML/min, 0.1 ML/min and 1.5 ML/min is 68.3°, 70.9° and 72.7°, respectively.

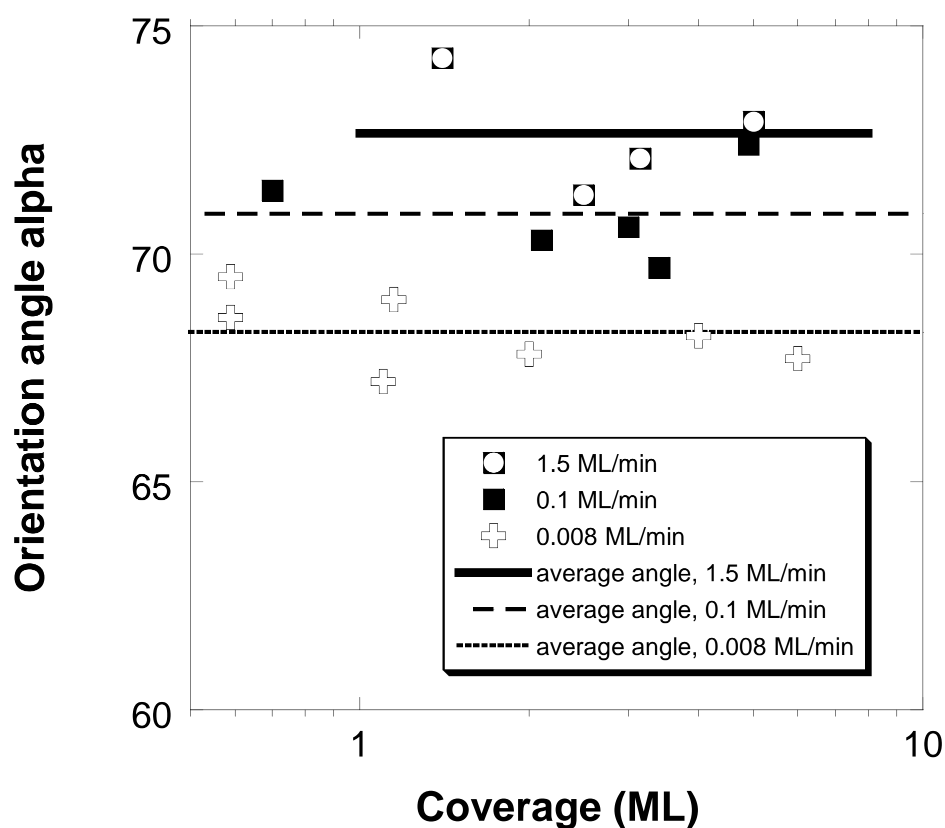

Fig. 3.5: The angle α versus coverage for pentacene films grown at three deposition rate. The straight line represents the average orientation angle for each deposition rate.

The other explanation for the dependence of α on the deposition rate is that only the 'thin film' and the 'bulk' phases exist and the ratio between two phases depends on the deposition rate. These two phases start to form at the initial stage of growth on the substrate. This interpretation is consistent with the previously reported that the bulk phase and thin film phase coexist as early as the first monolayer [3].

Based on this explanation, the average angle α from the three different deposition rates can be converted into the percentage of the thin film and the bulk phase. This two-phase model consists of a mixture of a thin film phase with a large layer spacing, 1.54 nm, with bulk phase in which the spacing is 1.45nm [2, 11]. From the length of the pentacene molecule (1.601 nm), the tilt angle α of the thin flim phase (74.1°) and the bulk phase (64.9°) can be calculated assuming α=γ (β=90°) in Fig. 3.1. The average angle <α>, weighted by the ratio of the mass of the molecules in each phase, is given by:

$$<\alpha>=\frac{M_{TF}}{M_{TF}+M_B}\times 74.1°+\frac{M_B}{M_B+M_{TF}}\times 64.9° \tag{3.2}$$

M_B and M_{TF} are the mass of the bulk phase and the thin film phase, respectively. The value of M_B/M_{TF} indicates the ratio of the bulk phase to the thin film phase. M_B/M_{TF} can be obtained from the experimental values of <α> at different deposition rates (Fig. 3.5). The result is shown in Fig. 3.6. The lower deposition rate leads to a higher fraction of the bulk phase. The effect of the deposition rate on the fraction of the film in each phase is pronounced at the very low deposition rate.

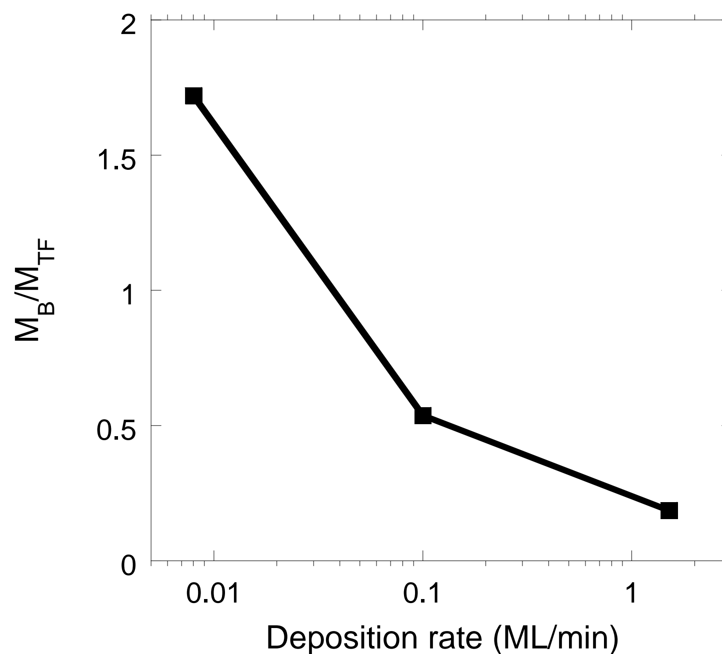

Fig. 3.6: Ratio of bulk phase to thin film phase versus deposition rate. The ratio was calculated from the average tilt angles $<\alpha>$ at different deposition rates indicated by horizontal lines in Fig. 3.5.

3.5 Conclusions

NEXAFS enabled us to probe the molecular orientation of the submonolayer pentacene which is very surface sensitive and determines the charge transport depending on its structural properties. Our work extended the structural information from x-ray diffraction measurements to a monolayer. The structure of pentacene films at very low coverage depends on a deposition rate and the structural difference between pentacene films can change the electrical properties of pentacene films in OFETs. The models we propose can

provide insight in relating transport of carriers in organic semiconductors to structural properties using OFETs. The combination of electrical characterizations of organic semiconductors using OFETs and the study of the orientation of molecules close to gate dielectric can provide a model system to optimize OFETs.

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Chapter 4

Functional Self-Assembled Monolayers and Photoinduced Charge Transfer in Organic Field Effect Transistors

4.1 Introduction

Creating and characterizing functional interfaces provides opportunities in incorporating new effects in electronic devices, such as OFETs, OLEDs and OPVs. The interfaces between metal contacts and organic semiconductors in OFETs and OLEDs have been extensively modified to control the molecular energy levels at the interfaces, which can change the energetic barriers for charge injection [1-4]. Self-assembled monolayers (SAMs) of organosilane molecules with permanent dipole polarization attached to the gate dielectric in OFETs were used to modulate the charge carrier density in organic semiconductors [5, 6].

OPVs have interfaces at which photoinduced charge transfer occurs. In these devices, the interface between electron donor and acceptor layers has a crucial role in determining the power conversion [7]. A number of studies have reported strategies for increasing the number of electrons transferred to the acceptor layers under illumination [7, 8]. Photoinduced charge transfer onto polymers to C_{60} molecules has been reported for a variety of polymers [10-13]. Bulk heterojunction material including C_{60} have been used to

make donor-acceptor interfaces for photovoltaic cells [14, 15]. In those studies, the bulk composites make it difficult to probe photoinduced charge transfer at the interface between electron donor and acceptor due to the small exciton diffusion length in organic semiconductors [16-20]. This diffusion length ranges from 3 to 15 nm and sets the fundamental length scale for studies of these interfaces.

Photoinduced charge transfer effects can be created by tailoring the interface between the organic semiconductors and the gate dielectric in OFETs. Here, we demonstrate that nanometer-scale electron acceptor layers incorporated in FETs provide structurally and electrically well defined interfaces at which photoinduced charge transfer can be observed and studied quantitatively.

A surface with a large number of electron acceptors can be made by affixing an amine-terminated self assembled monolayer (SAM) to an SiO_2 surface and subsequently functionalizing it with C_{60}. This interface can be created on top of SiO_2 gate dielectric of an OFET, and incorporated in an operating device. The threshold voltages in pentacene FETs deposited onto these functionalized interfaces can be measured under conditions of varying illumination.

Kobayashi *et al.* demonstrated that the charge density can be controlled by introducing SAMs with a high dipole moment between pentacene and SiO_2 [5]. The dipole moment between the gate insulator and organic semiconductors in FETs can modulate the charge density and cause a shift in the threshold voltage due to a built in electric field. The built in electric field changes the surface potential and results in the same effect as applying a gate voltage. The built in electric field can be expressed as:

$$E_{in} = N\left(\frac{\mu_{mol}}{\varepsilon\varepsilon_0 d_{mol}}\right) \tag{4.1}$$

Here, N and d_{mol} are the areal density and molecular length of SAM, respectively. ε represents the dielectric permittivity of SAMs and ε_0 is the vacuum permittivity [6].

In our study, the functionalized interfaces were characterized with spectroscopic techniques. The electrical signatures of photoinduced charge transfer at the interface can be found by measuring the threshold voltage in the dark and under illumination. The threshold voltages of pentacene FETs with C_{60} electron acceptors allow the number of electrons trapped into C_{60} molecules under illumination to be measured. The number of electrons trapped into the C_{60} molecules depends on the photon flux at a particular wavelength and the gate electric field. The shift in the threshold voltage under illumination will be discussed relating to the amount of C_{60} molecules at the interface.

4.2 Experimental methods

Two deposition steps are needed to make the functionalized self assembled monolayers (SAMs). 3-aminopropyltriethoxysilane (APTS) SAMs were attached to the silicon dioxide substrate. The substrate was immersed in a solution of 94% acidic methanol (1.0 mM acetic acid in methanol), 5% H_2O, and 1% APTS for 15 min at room temperature. All percentages were in volume per volume. The substrate was then rinsed in methanol. The amine-terminated SAMs were baked on a hot plate at 120°C for 5 min. To remove physisorbed amine molecules we immersed the sample in an ultrasonic bath for 2 min and then rinsed the substrate in methanol.

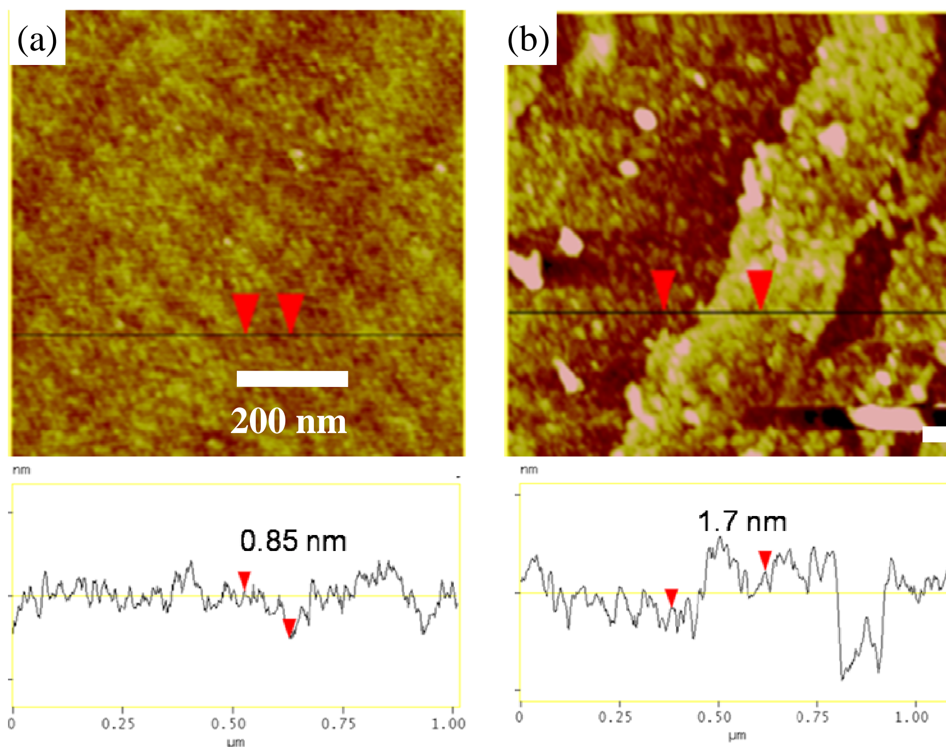

Fig. 4.1: AFM images of (a) an amine-terminated SAM and (b) a C_{60}- terminated SAM.

To attach C_{60} molecules to the APTS SAMs, the amine terminated substrate was exposed to a 1 mM solution of C_{60} in toluene for 3 days at 80°C. The functionalization proceeded through an N-H addition reaction across the C=C bonds in C_{60} resulting in the fusion of two six-membered rings [21]. The substrate was rinsed in toluene to remove the residual physisorbed C_{60} molecules. After attaching C_{60} molecules to the amine-terminated SAM, sample became more hydrophobic. The contact angle for water on the amine-terminated surface was 49°. The contact angle for the C_{60}-terminated surface rose to 82°. A similar increase was reported in the original studies of these monolayers by Chen *et al.* [21].

Fig. 4.1 shows AFM images of an amine-terminated SAM and C_{60}-terminated SAM on the SiO_2 surface. The AFM line scan for the amine-terminatd SAM Fig. 4.1(a) shows that the height of the clusters on the surface, which appear as bright spots in the AFM image was 0.85 nm. This height is consistent with the molecular length of the amine-terminated SAM [22]. After attaching a C_{60}-terminated SAM the roughness was increased from 0.25 nm to 1.93 nm.

The amine-terminated SAM on the SiO_2 surface was examined using x-ray photoelectron spectroscopy (XPS). We observed a N (1s) peak at 400.2 eV in photoelectron spectra due to the –NH group of the amine-terminated SAM [23].

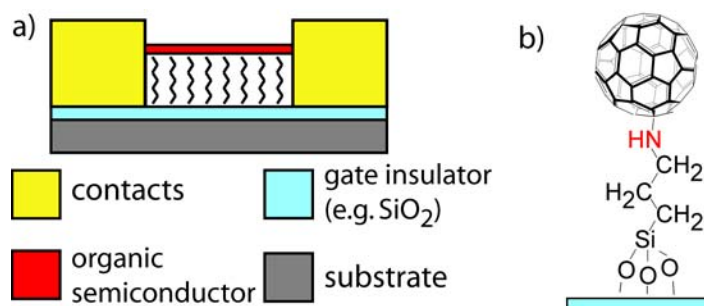

Fig. 4.2: Schematic diagrams of (a) an FET incorporating the acceptor-terminated monolayer at the interfaces between organic semiconductor and the gate dielectric and (b) C_{60}-terminated SAM attached to SiO_2.

Bottom contact FETs were fabricated using the process described in Chapter 2. After the SAMs were deposited onto the FETs, they were loaded in a vacuum chamber and pumped down to the working pressure of 2×10^{-6} torr. Pentacene was deposited onto the

functionalized self assembled monolayers at a deposition rate of 0.7 ML/min. The thickness of the pentacene film was approximately 30 nm.

Fig. 4.2(a) shows the geometry of the transistor device we used in this experiment. The channel length used in the electrical measurements ranged from 15 μm to 40 μm and the width was 1 mm. Fig. 4.2(b) displays the schematic diagram of C_{60}-terminated SAM. Transistors on unfunctionalized silicon dioxide surfaces were used as control samples to clarify a role of the functionalized self assembled monolayers in charge transfer.

4.3 Threshold voltage shifts by dipole field effect

We repeated the experiments of Kobayashi *et al*. to determine whether the direction of the shift in the threshold voltage due to a fluorinated SAM is consistent with the direction of the molecular dipolar moment of the SAM. The immobilization of the fluorinated molecules (1H,1H,2H,2H-perfluorooctyl-trichlorosilane) onto the SiO_2 surface was carried out by dipping FET devices into a solution of the SAM molecules in toluene at 80°C for 1 day. In the AFM images of Fig. 4.3(b), the rms roughness of the fluorinated surface was 1.3 nm, which shows that some of the molecules formed clusters on the surface. The AFM image of the surface with the fluorinated SAM in Fig. 4.3(b) shows that the heights of the clusters were much larger than the molecular length of 1~2 nm [5].

Two samples were prepared to investigate the effect of the fluorinated SAM on the threshold voltage of the pentacene FETs. One was a control sample without the flourinated SAM and the other had a fluorinated SAM attached to the SiO_2 substrate. After the deposition of a 100 nm-thick pentacene layer, the current-voltage characteristics of both devices were measured.

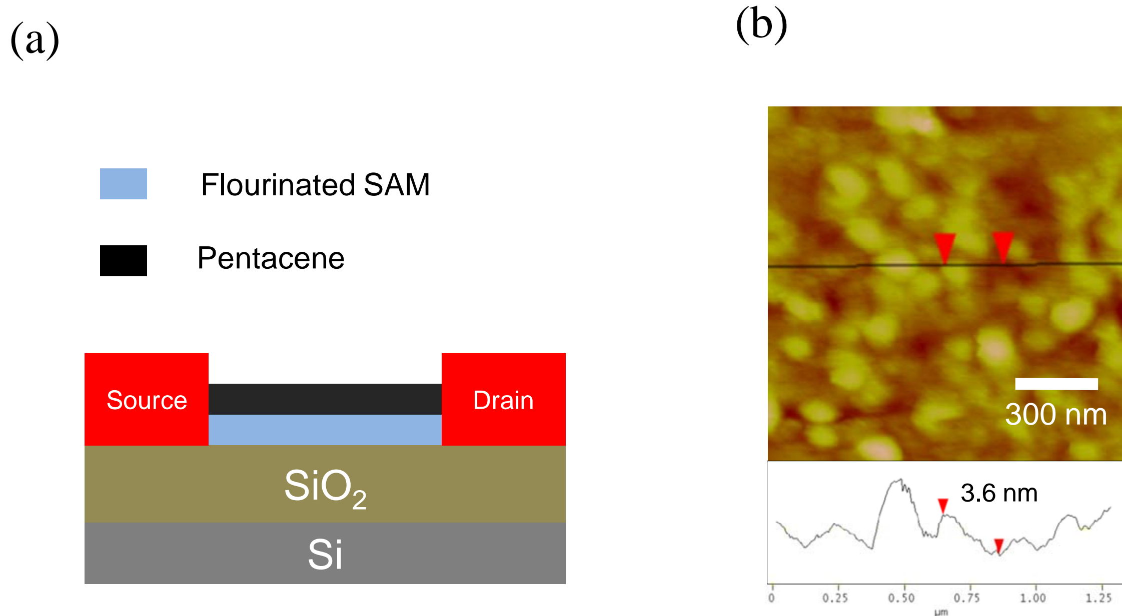

Fig. 4.3: (a) A schematic diagram of a pentacene FET fabricated with a fluorinated SAM on the SiO_2 gate dielectric. (b) AFM images of a fluorinated SAM before depositing pentacene.

For the control sample, the turn-on voltage was in the range between -10 to 10 V. The turn-on voltage is discussed here instead of the threshold voltage because the turn-on voltage can be measured more easily in the gate voltage versus drain current plot. In a plot of the log of the drain current, the turn-on voltage is the gate voltage at which onset of current is observed. Threshold voltage is flat band voltage in OFETs that operate in an accumulation mode. In some cases the threshold voltage does not coincide with the turn-on voltage. According to Pernstich *et al.* [24], the difference between the turn-on voltage and

the threshold voltage is due to the traps at the interface between gate dielectric and organic semiconductors. As the gate voltage increases more of these traps are occupied by carriers. Finally the traps are filled with carriers induced by increasing gate voltage and the threshold voltage is reached. At the turn on voltage, the channel is depleted and the source-drain current is very small. The turn on voltage of pentacene deposited on fluorinated SAM was 45 V in Fig. 4.4.

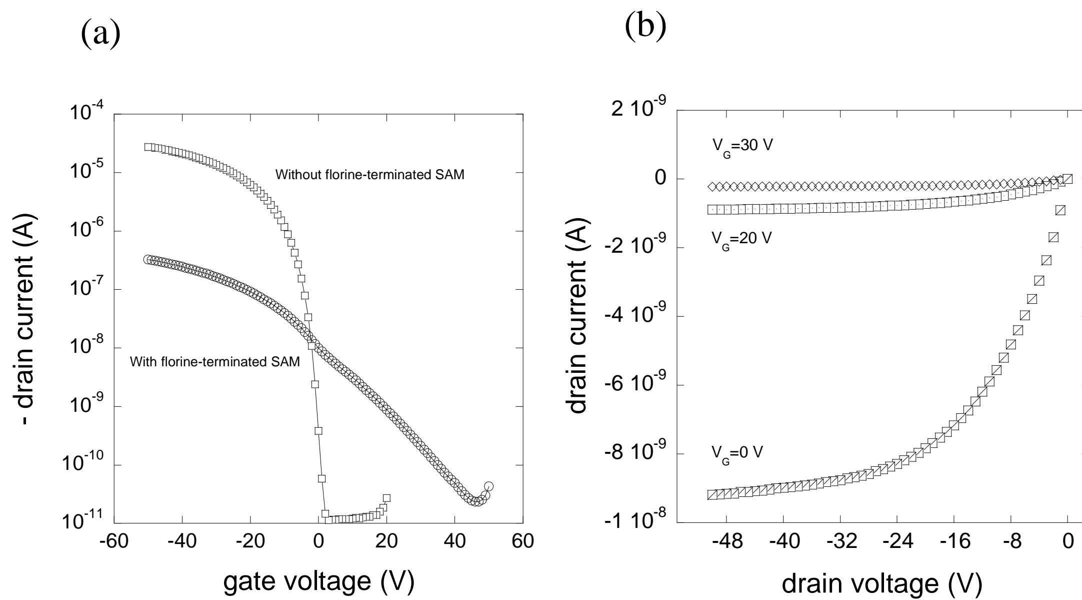

Fig. 4.4: (a) Transfer characteristic curves of pentacene FETs with and without the fluorinated SAM. (b) Output characteristic curves of a pentacene FET with fluorinated SAM.

The turn-on voltage of the pentacene FET shifted to more positive value after attaching the fluorinated SAM to the SiO_2 gate dielectric. In Fig. 4.4(a), the fluorinated SAM with a high dipole moment accumulated holes in the pentacene layer by the built in electric field arising from the fluorinated SAM. The dipole moment of the fluorinated molecule is 2

Debye and the length of the molecule is 1.3 nm [5]. The predicted value of the threshold voltage shift based on equation 4.1 was 230 V. This value is based on the assumption that the SAMs are uniformly deposited and the area density of molecules in the SAM is $2\times10^{14}cm^{-2}$. The experimental value of the threshold voltage is much lower than the theoretically expected value. The difference could arise from disorder in the layer of flourine molecules, which would reduce the average dipole moment in comparison with the uniformly deposited layer.

The output characteristic curves in Fig. 4.4(b) show that hole current flows in the pentacene layer even at high positive gate voltages. At these voltages there are no mobile carriers in a device without the fluorinated SAM. At V_G=20 V, the drain current increased proportional to the drain voltage and saturated at higher drain voltage. This behavior is typical of *p*-type OFETs [25]. This indicates that holes are induced in the pentacene layer at positive gate voltage due to the built-in electric field of the fluorinated SAM pointing toward the pentacene layer.

We illuminated a pentacene FET sample with a fluorinated SAM with an incandescent light. The current-voltage characteristic curve in Fig. 4.5 shows that the turn-on voltage did not change under illumination. This indicates that the incandescent light did not change the carrier density in the pentacene layer. There was no signature of any change in the fluorinated SAM resulting in a change in the built-in electric field. There was also no sign of photoinduced charge transfer between the fluorinated SAM and pentacene.

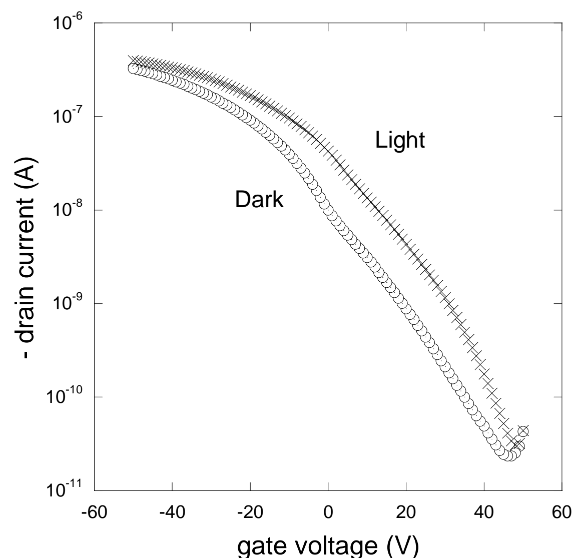

Fig. 4.5: The effect of illumination on the current voltage characteristics of a pentacene FET fabricated on a gate dielectric with a flourinated SAM. Current-voltage characteristics were recorded in the dark and during illumination with an incandescent light. The source-drain voltage was -50 V.

4.4 Threshold voltage shifts due to photoinduced charge transfer

The effect of light on the threshold voltage of a FET formed on an SiO_2 gate dielectric functionalized with an amine-terminated SAM and C_{60} molecules is shown in Fig. 4.6(a). In the dark, the turn-on voltage of the pentacene FET fabricated on SAMs with amine-terminated layer alone was close to -10 V. The control samples on bare SiO_2 gate dielectrics had a threshold voltage with a magnitude of less than 10 V in repeated experiments. These small threshold voltages are consistent with previous observations in

the literature [24, 26]. The turn-on voltage obtained for a pentacene FET on the amine-terminated SAM is consistent with a low dipole moment predicted for the amine-terminated SAM [5]. Assuming that the areal density of molecules in the amine-terminated SAM is $2\times10^{14}/cm^2$ and that the length is 1 nm, the built-in electric field calculated from equation 4.1, E_{in}, is 4.5×10^5 V/cm. This built-in electric field is the same as applying the gate voltage of -9 V across the 200 nm SiO_2 gate dielectric. A gate voltage of +9 V across the 200 nm SiO_2 gate dielectric would be necessary to compensate the surface potential caused by the amine-terminated SAM. Under illumination with the incandescent light, the turn-on voltage shifted in the positive by 10 V.

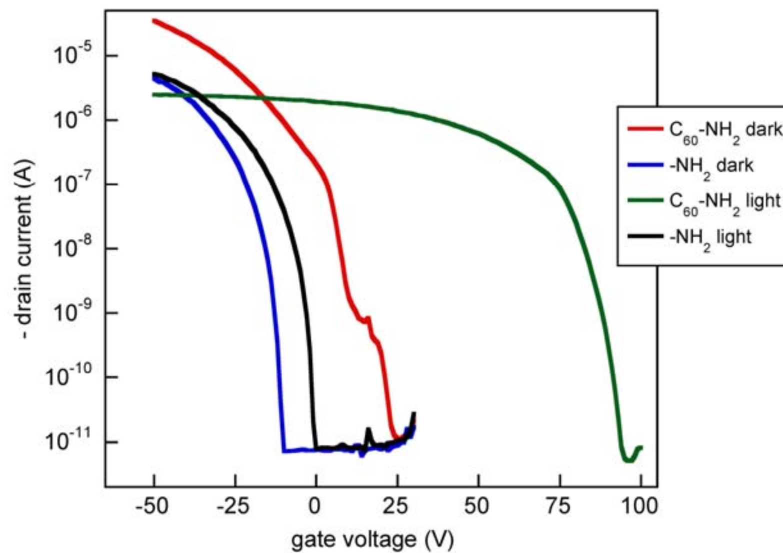

Fig. 4.6: Transfer characteristic curves in the saturation regime (V_D=-50 V) of a pentacene FET in which the SiO_2 gate dielectric has been functionalized with an amine-terminated SAM and C_{60}-terminated SAM. An incandescent light source was used for the illumination. The curves are labeled with the surface preparation and illumination conditions.

The attachment of C_{60} molecules to the amine-terminated SAM causes a large change in the charge density in the pentacene layer during illumination. This effect results in a large shift in the threshold voltage of the FET. The threshold voltage shifted from 6 V to 90 V during illumination with an incandescent light in Fig. 4.6. The shift in the threshold voltage can be converted to the number of charges transferred to C_{60} molecules by assuming that the threshold voltage is the voltage at which the total charge in the pentacene is zero. With this assumption, the charge Q transferred to the C_{60} layer is given by:

$$Q = C_{gd} V_G \tag{4.2}$$

The change in the threshold voltage by 84 V corresponds to the transfer of 9×10^{12} charge carriers per cm^2 to C_{60} molecules According to Chen *et al*. the areal density of a close packed layer of C_{60} molecules on an amine terminated SAM is 1.1×10^{14} molecules per cm^2 [21]. Since the charge density transferred to the C_{60} layer in our experiments was far less, 9×10^{12} charge carriers per cm^2, either C_{60} molecules have not been completed on the amine-terminated SAM or incomplete coverage of an amine-terminated SAM.

The role of the C_{60}-terminated SAM in changing the threshold voltage of the pentacene FET can be explained qualitatively using energy band diagrams. Fig. 4.7 shows schematic energy band diagrams for pentacene FETs with and without C_{60}-terminated SAMs. In Fig. 4.7(a), the pentacene FET without C_{60}-terminated SAM is at the flat band condition. When a negative voltage is applied to the highly doped p-type Si the Fermi level of the gate electrode goes up (Fig. 4.7(b)). The highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) level bend upwards by applying a negative voltage. Mobile holes are accumulated at the interface between pentacene and SiO_2 and

form the conducting channel. A positive gate voltage depletes holes in the pentacene layer close to SiO_2 (Fig. 4.7(c)).

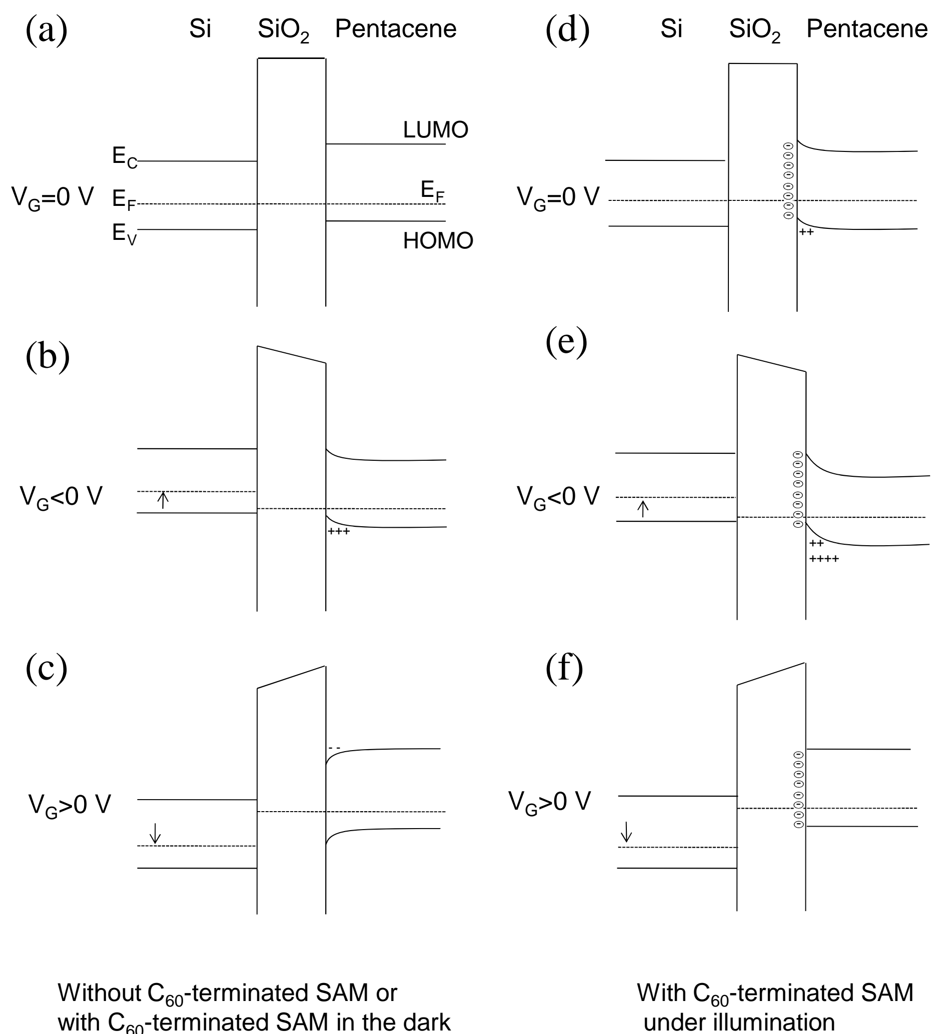

Fig. 4.7: Schematic energy band diagrams for pentacene FETs at different bias conditions. (a) V_G=0 V, (b) V_G<0 V, and (c) V_G>0 V for pentacene FETs without C_{60}-terminated SAMs. (d) V_G=0 V, (e) V_G<0 V, and (f) V_G>0V for pentacene FETs with C_{60}-terminated SAMs under illumination. A highly doped p-type Si was used as a gate electrode.

For the pentacene FETs with C_{60}-terminated SAMs, mobile holes are present in the pentacene layer at zero gate voltage under illumination (Fig. 4.7(d)). Photogenerated electrons from the pentacene layer are trapped in the surface states produced by C_{60} molecules. The trapped electrons cause the LUMO and HOMO level to bend upwards and induce holes in the pentacene layer at zero gate voltage. The trapped electrons have the same effect as applying a negative gate voltage. A negative gate voltage applied to the device accumulates more holes than in pentacene FETs without C_{60}-terminated SAMs (Fig. 4.7(e)). In Fig. 4.7(f), the trapped electrons on C_{60} molecules make the LUMO and HOMO level of pentacene at the interface flat. This makes it possible to accumulate holes in the pentacene layer even at a positive gate voltage resulting in the shift in the threshold voltage toward the positive.

4.5 Light intensity effect on threshold voltage shifts

The charge transfer process can be understood more clearly using a light source with a single wavelength. Drain current-voltage characteristic curves for pentacene transistors on C_{60}-teminated SAMs are shown in Fig. 4.8(a). The characteristics were acquired in the linear regime of transistor operation. We illuminated the FETs at a series of intensities up to 7.5 mW/cm^2 using a laser diode with a wavelength of 650 nm. Threshold voltage was measured at each intensity in Fig. 4.8(a) and plotted as a function of light intensity in Fig. 4.8(b). In Fig. 4.8(b), the threshold voltage increases almost linearly depending on the laser intensity and saturates.

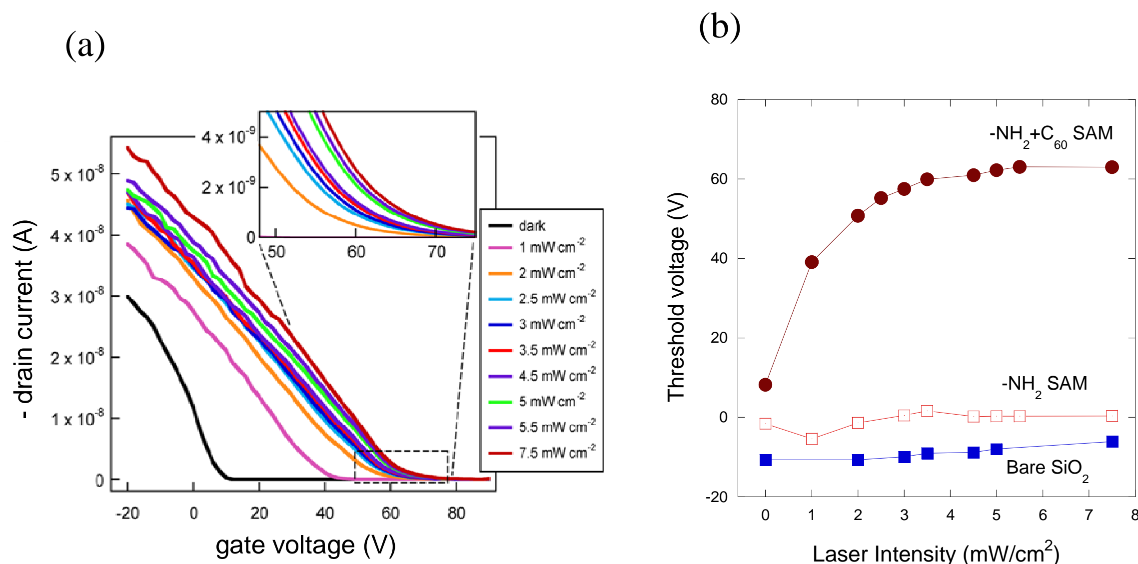

Fig. 4.8: (a) Transfer characteristic curves in the linear regime, with V_D=-3 V, for a pentacene FET on a C_{60}-terminated SAM acquired as a function of the intensity illuminated at 650 nm wavelength. (b) Threshold voltage of pentacene FETs as a function of the light intensity.

For the control samples fabricated on bare SiO_2 and on an amine-terminated SAM, the change in the threshold voltage during illumination was negligible. However, for the pentacene FET on the C_{60}-terminated SAM, the threshold voltage shifted towards more positive values with increasing light intensity.

As the light intensity increased the concentration of electrons transferred to the C_{60}-terminated SAM increased, resulting in a larger shift in the threshold voltage. The saturation of the threshold voltage for high light intensities suggests that the charge transfer process was saturated due to the limited number of C_{60} molecules available at the interface.

4.6 Gate electric field effect on threshold voltage shifts

Gate electric field has a large effect on the shift in the threshold voltage under illumination. Fig. 4.9 shows transfer characteristic curves for a FET device with pentacene on the C_{60}-terminated SAM, in the dark and under illumination. The thickness of pentacene layer is 40 nm. The most important aspect of the measurements in Fig. 4.9 is that the electrical characteristics were recorded for two different directions of the scan of the gate voltage. In the dark, the threshold voltage was independent of the direction of the gate voltage sweep. The threshold voltage measured in the forward sweep from 60 V to -30 V was 1.3 V which is almost the same as -0.3 V obtained from the reverse sweep from -30 V to 60 V.

Under illumination, the magnitude of the shift in the threshold voltage depended on the direction of the scan. During the scan from negative gate voltage to positive gate voltage, the threshold voltage was 10 V. In the sweep from positive gate voltage to negative gate voltage, the threshold voltage was 36 V. The change in the threshold voltage shift arising from the sweep direction during illumination was 26 V. The number of electrons trapped on C_{60} molecules in the scan from negative voltage to positive voltage was decreased by 2.8×10^{12} electron cm^{-2} in comparison with that in the sweep direction from positive gate voltage to negative gate voltage based on equation 4.2. In a control sample where pentacene was deposited onto SiO_2 without the amine-terminated SAM or C_{60} molecules, we found that the threshold voltage change was negligible and the threshold voltage was independent of the sweep direction under illumination.

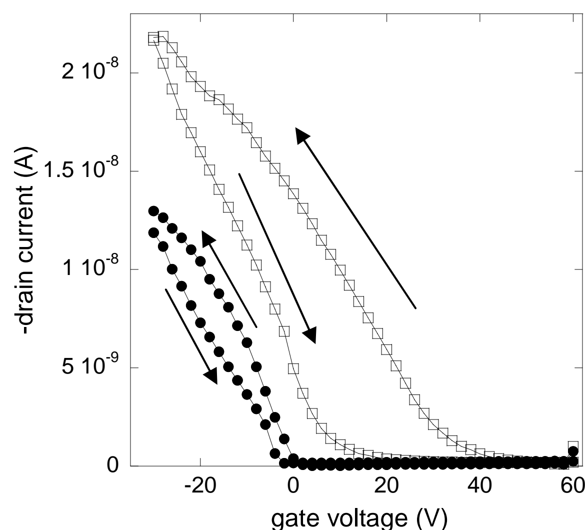

Fig. 4.9: Characteristic curves of a C_{60}-functionalized FET in the dark (filled circles) and under illumination with a 650 nm laser diode at an intensity of 3 mW/cm^2 (open squares).

Fig. 4.10 shows that the magnitude of the gate voltage changes the magnitude of the shift in the threshold voltage during illumination. While illuminating a pentacene FET sample with C_{60}-terminated SAM at a constant light intensity of 3 mW/cm^2 we varied the range of the gate voltage scan. The starting range was 0 to -20 V. In this range of the gate voltage scan, current-voltage characteristics were obtained in the dark and under illumination. We then made a series of scans in which the final voltage ranged from -20 to 80 V. These measurements were performed in the linear regime.

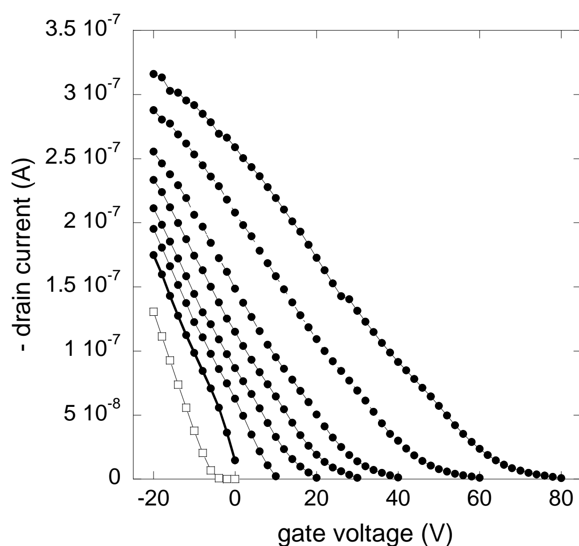

Fig. 4.10: Transfer characteristic curves measurements were recorded for a number of ranges of the gate voltage scan in the dark (open squares) and under illumination with a 650 nm laser diode (filled circles). The drain voltage was at -3 V.

Range of gate voltage scan	Threshold voltage (V)
0 V to -20 V (dark)	-5.9
0 V to -20 V (light)	3.7
10 V to -20 V (light)	9.8
20 V to -20 V (light)	16
30 V to -20 V (light)	22
40 V to -20 V (light)	29
60 V to -20 V (light)	43
80 V to -20 V (light)	60

Table 4.1: Threshold voltages of a C_{60}-functionalized pentacene FET for different ranges of the gate voltage scan.

As summarized in Table 4.1, scan ranges starting at more positive gate voltages led to a larger shift in the threshold voltage. In the dark, the threshold voltage was -5.9 V, with a scan range from 0 to -20 V. During illumination the threshold voltage shifted to 3.7 V for the same gate voltage scan. The difference in the threshold voltage, 10 V, shows that 1.1×10^{12} electrons cm^{-2} were trapped on C_{60} molecules based on equation 4.2. In the dark, the threshold voltage was independent of the scan range. When gate voltage was scanned from 80 to -20 V the threshold voltage was changed by 66 V in comparison with that for the range of scan from 0 to -20 V in the dark. This change in the threshold voltage indicates that 7.1×10^{12} electrons cm^{-2} were trapped on C_{60} molecules, which is 7 times larger than in the dark. A larger positive gate voltage thus aids electron transfer to C_{60} molecules.

The effect of the gate electric field and the light intensity on photoinduced electron transfer can be quantified by measuring the number of electrons trapped in C_{60} after illuminating the system for a sufficient time to reach equilibrium. This method was described by Podzorov *et al*. [27]. In our experiment, the FET samples were illuminated while applying a gate voltage, $V_{G,illumination}$, for 5 min. at a particular light intensity. We then turned off the light and stopped applying voltages at the same time. To measure the threshold voltage gate voltage was scanned from 80 to -20 V in the dark. In Fig. 4.11, the threshold voltage is plotted as a function of light intensity for two different values of the gate voltage during illumination, $V_{G,illumination}$. The threshold voltages of the FET at $V_{G,illumination}$=30 V and 90 V under illumination with a light intensity of 3 mW/cm^2 are 11 V and 28 V, respectively. At a constant $V_{G,illumination}$, the threshold voltage increased as the light intensity increased and saturated at high light intensities. A larger value of the

saturated threshold voltage shift was observed at higher $V_{G,illumination}$.

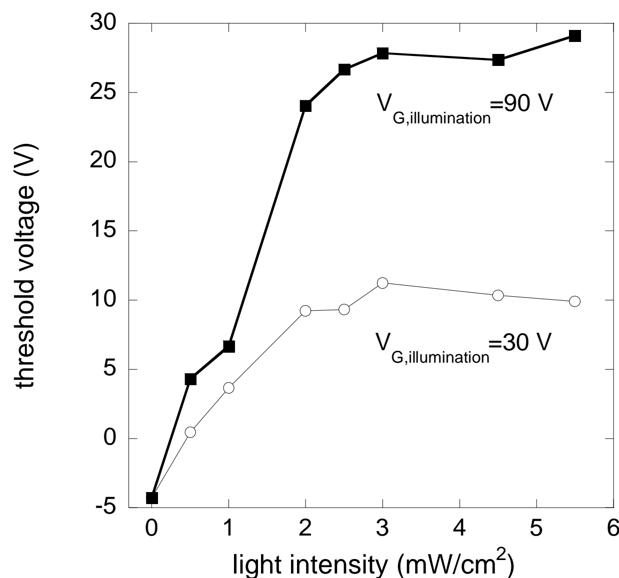

Fig. 4.11: Threshold voltage as a function of light intensity measured for two different gate electric fields. Gate voltages of 30 V (open circles) and 90 V (filled squares) were applied to a pentacene FET on a C_{60}-terminated SAM for 5 min. during illumination.

4.7 Reversibility of photoinduced charge transfer

Reversibility of charge transfer at the interface between pentacene and C_{60} molecules during illumination can be checked by monitoring drain current as a function of time at the beginning and end of illumination. Drain current in the linear regime is expressed by:

$$I_D = \frac{W}{L}\mu C_{gd}(V_G - V_T)V_D \tag{4.3}$$

In the equation, drain current increases as threshold voltage increases at constant gate and

drain voltage. The change in the threshold voltage in response to light is thus reflected by the change in drain current.

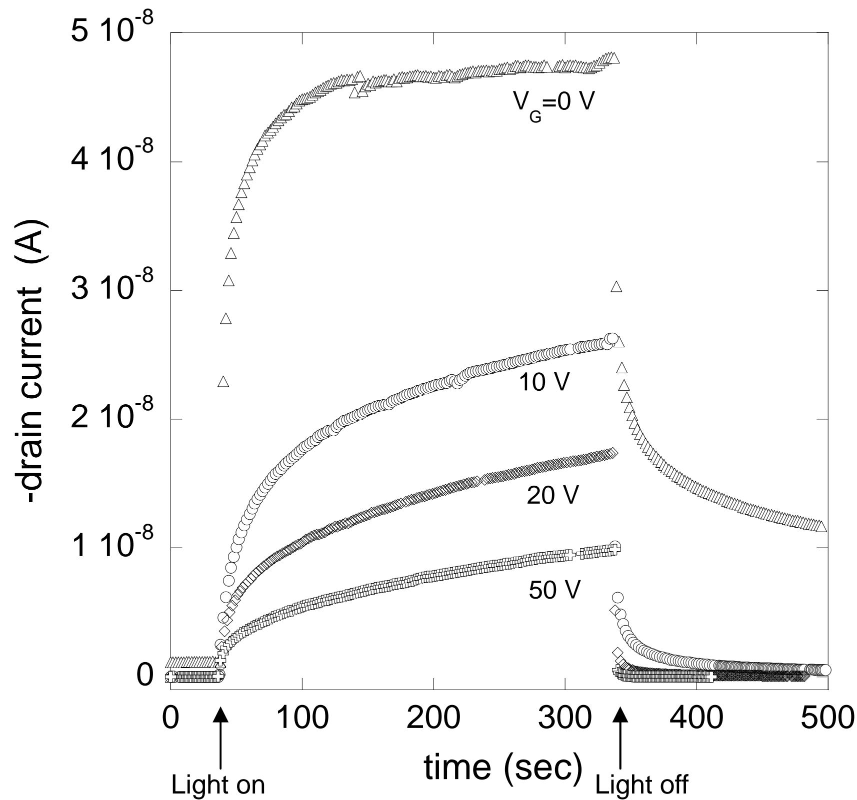

Fig. 4.12: Drain current as a function of time for gate voltages of 0, 10, 20 and 50 V. A 650 nm laser diode with a light intensity of 3 mW/cm^2 was used as the light source. The drain voltage was -3 V.

The drain current is plotted as a function of time in the dark and under illumination in Fig. 4.12. The drain current was recorded at a constant gate and drain voltage throughout these measurements. In Fig. 4.12, the drain current less than 20 pA was observed at gate voltages

of 10, 20 and 50 V in the dark before illumination. In the dark, the transfer characteristic curve of a pentacene FET sample with a C_{60}-terminated SAM showed that the threshold voltage was +5 V. The drain current at gate voltages of 10, 20 and 50 V in the dark was small because there were no mobile charge carriers in the pentacene under these conditions. Immediately after the light was turned on, the drain current began to increase for all the gate voltages. The drain current continued to increase with time during illumination, which suggests that electrons are being trapped in C_{60} leading to a change in the threshold voltage.

When the light was turned off the threshold voltage shifted to the negative and the drain current decreased. The drain current fell to 60 pA in 10 seconds in the dark at the gate voltage of 50 V. In 60 seconds after light was turned off the drain current was 10 pA which is close to the value before illumination. The electrons trapped in the C_{60}-terminated SAM during illumination returned to the pentacene in the dark, resulting in the shift of the threshold voltage towards zero. Charge transfer between C_{60} and pentacene during illumination is thus reversible in response to light.

4.8 Growth of pentacene on functionalized surfaces

The functionalized self assembled monolayers on SiO_2 also change the growth of pentacene thin films. The rms surface roughness of the amine-terminated SAM is 0.15 nm (Fig. 4.13(a)). Adding the C_{60} increases the rms surface roughness to 0.29 nm. This is apparently due to the formation of clusters of C_{60} on the surface (Fig. 4.13(b)), in addition to the uniformly distributed C_{60} layer discussed by Chen *et al.* [21].

Pentacene thin films deposited on these surfaces form islands that grow in three dimensions immediately (Fig. 4.13(c)), whereas pentacene thin films on the SiO_2 surface produce larger grains (Fig. 4.13(d)). Furthermore, while islands in the first layer of pentacene thin films on SiO_2 come into contact with each other before the second layer begins to form, as shown in chapter 2, islands on the C_{60}-terminated SAM grow into multiple layers immediately. A relatively large average thickness of pentacene in films on the C_{60}-terminated SAMs is required to form films in which the islands are electrically connected.

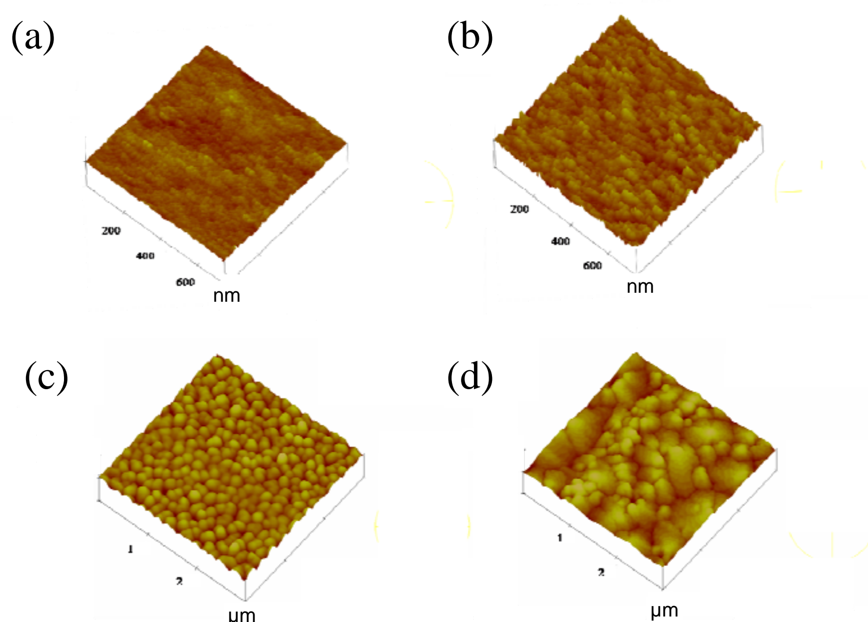

Fig. 4.13: AFM images of (a) an SiO_2 surface functionalized with an amine-terminated SAM, (b) a C_{60}-terminated SAM, (c) pentacene deposited on C_{60}-terminated SAM and (d) pentacene on SiO_2

The change in the growth of the pentacene films influences on the electrical properties of FETs fabricated on C_{60}-terminated SAMs. Thicker pentacene films are required to achieve hole mobilities comparable to those of pentacene deposited on SiO_2 substrates without SAMs. The saturation mobilities for pentacene FETs on SiO_2 substrate and on the C_{60}-terminated SAM were 0.09 cm^2/Vs and 3.6×10^{-4} cm^2/Vs, respectively at pentacene thicknesses of approximately 10 nm. Adding more pentacene to the C_{60}-terminated SAM improved the contacts between pentacene islands and this resulted in the rapid increase of the mobility to 0.09 cm^2/Vs. Adding pentacene to the functionalized SiO_2, which already formed a completed layer near the gate insulator, did not change the mobility.

4.9 Conclusions

The sensitivity of the accumulation layer to the interface between the gate dielectric and organic semiconductors in OFETs made it possible to probe the electronic structure of the functionalized gate dielectric surface. This approach can be used to evaluate organic semiconducting materials that can be incorporated into organic solar cells and take part in photoinduced charge transfer. Electronic structures of the interfaces organic semiconductors form with a variety of inorganic surfaces can be studied using this approach.

4.10 References

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Chapter 5

Self-assembled Dipolar Chromophores in Organic Field Effect Transistors

5.1 Introduction

Chromophores with donor and acceptor groups linked by alternating single and double bonds have had many uses in non-linear optical and electro-optic applications [1-3]. The chromophores routinely have a high electric dipole moment [2]. The magnitude of the dipole moment can be changed reversibly by illuminating the molecules. The tunable dipole moment of the chromophores can affect the current-voltage characteristics of OFETs by changing the conductivity of organic semiconductors on which the chromophores are deposited. DR19 is an azobenzene-based chromophore with a high dipole moment (~8 Debye) [1]. Azobenzene consists of two phenyl rings connected by a N=N double bond.

Here, we use a SAM of dipolar chromophores with a large dipole moment at the interface between the gate dielectric and organic semiconductor to alter the carrier density in the channel of the FET. The internal changes of the DR19 molecules by light at the interface can be detected using the current-voltage characteristics of pentacene FETs.

5.2 Experimental methods

Triethoxychlorosilane ($(C_2H_5O)_3SiCl_3$) groups were added to the DR19 in Padma Gopalan's lab. These groups allowed the DR19 to be attached to the surface of SiO_2. The

DR19 was immobilized on the SiO_2 gate dielectric of a FET device by soaking the device in a toluene solution with 2 mg of DR19 per ml of solvent at 90 °C [3]. The duration of this deposition will be discussed below. To form FET devices incorporating the functional layer, the DR19 was deposited onto a substrate with pre-patterned gold electrodes on SiO_2.

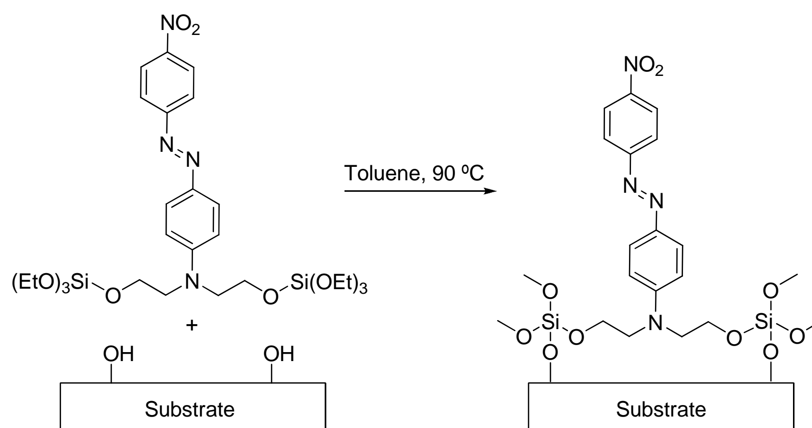

Fig. 5.1: Attachment of DR19 to SiO_2.

5.3 Structural characterization of DR19 on SiO_2 surface

The surfaces that had been exposed to DR19 were studied with X-ray photoelectron spectroscopy (XPS) and attenuated total reflection Fourier transform infrared spectroscopy (ATR-FTIR). Using XPS [Fig. 5.2], we observed N(1s) peaks corresponding to N=N, N, and NO_2 groups of the DR19 molecules and the peaks due to silicon and oxygen [4].

In Fig. 5.3, the ATR-FTIR spectra show a C-H stretch at 2890 cm^{-1}, a C=C mode at 1600 cm^{-1}, an asymmetric NO_2 stretch mode at 1514 cm^{-1}, a N=N mode at 1384 cm^{-1}, and a symmetric NO_2 stretch at 1338 cm^{-1} [4]. The combination of the XPS and ATR-FTIR results shows that DR19 layers were deposited on the SiO_2 substrate.

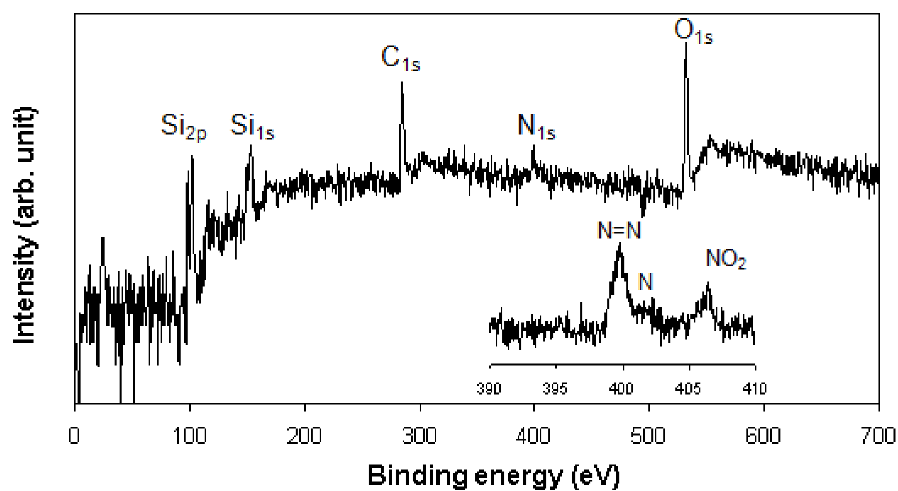

Fig. 5.2: XPS spectra of functionalized DR19 on SiO_2.

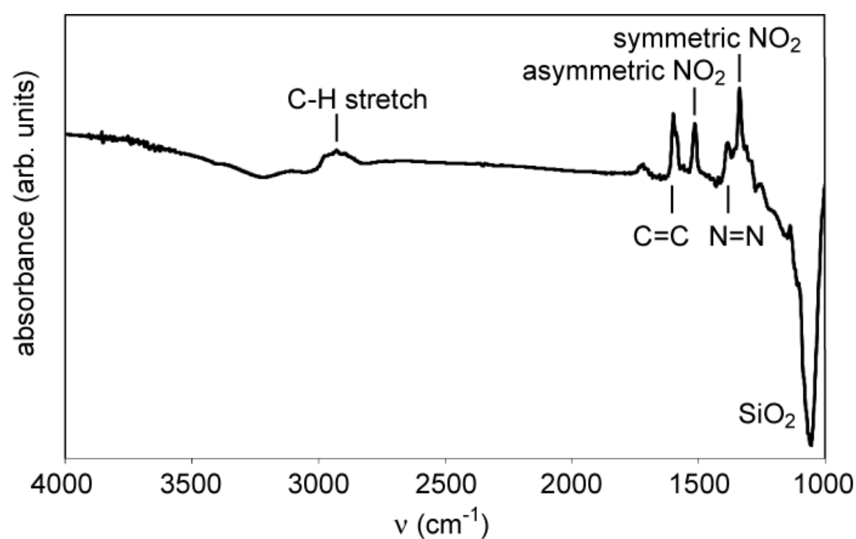

Fig. 5.3: ATR-FTIR spectra of DR19 on a Si substrate covered with the native oxide.

5.4 Threshold voltage shifts in FETs

Fig. 5.4(a) shows a schematic diagram of a device used to study the effect of DR19 on the threshold voltage of a pentacene FET. The thickness of the DR19 and pentacene layers

are 30 nm and 40 nm, respectively. The thickness of pentacene is calculated from the deposition rate we calibrated using AFM images and the deposition time at a particular temperature of the effusion cell. For the measurement of the thickness of DR19, we scratched the DR19 layers on SiO_2 and measured the height between the regions scratched and covered with the DR19 layer. Fig. 5.4(b) shows the effect of the illumination on the transfer characteristic curves of pentacene FETs on a DR19 layer on SiO_2.

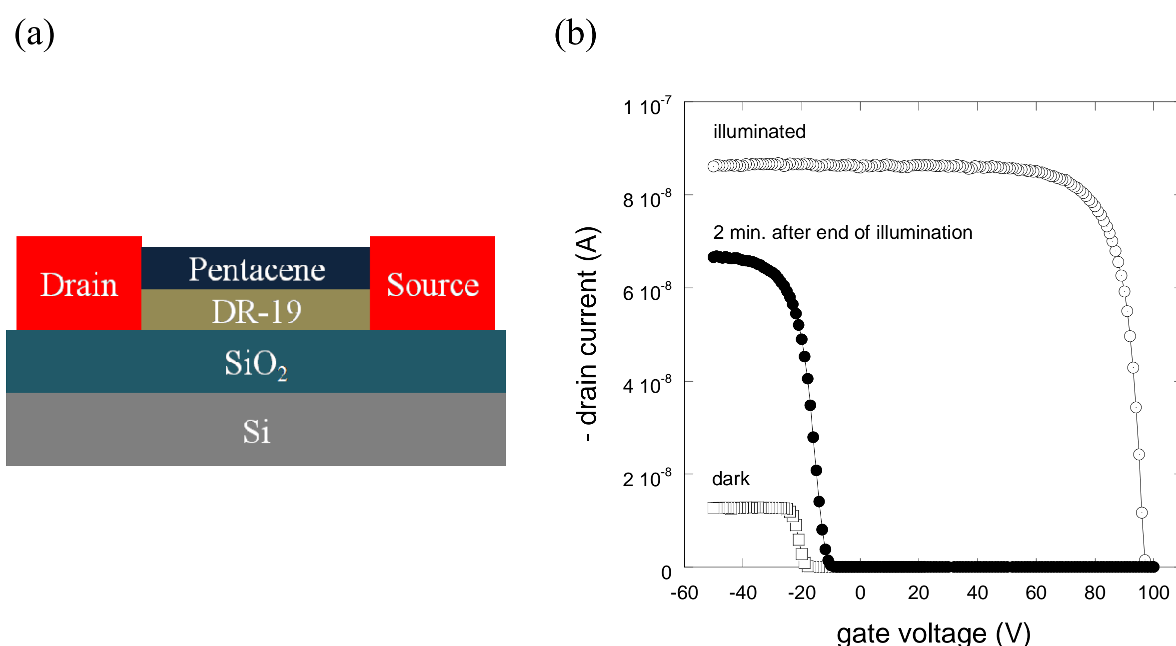

Fig. 5.4: (a) A schematic diagram of a pentacene FET on a DR19 layer on SiO_2. (b) Transfer characteristics of pentacene FET devices before and after illumination with a laser diode of 650 nm wavelength. The measurements were acquired in the linear regime of transistor operation with a drain voltage of -2 V. The gate voltage was scanned from 100 V to -50 V.

In Fig. 5.4(b), the drain current is plotted as a function of gate voltage in the linear regime of the transistor current voltage characteristics. The threshold voltage measured in the dark was -19 V. After the measurement in the dark, the sample was illuminated with a light intensity of 3 mW/cm^2 using a laser diode and the threshold voltage changed to +97 V. The threshold voltage in two minutes after the end of illumination was -13 V, which is very close to the initial value of -19 V. This indicates that the shift in the threshold voltage during illumination is reversible.

5.5 Effect of the light intensity on the threshold voltage shifts

The effect of the magnitude of the photon flux on the threshold voltage was studied for light intensities up to 5.5 mW/cm^2. Fig. 5.5(a) shows the drain current-gate voltage characteristic curves measured varying the light intensities for a pentacene FET with the DR19 layer.

The threshold voltage of the device in the dark was 9 V. Under illumination with laser intensity of 1 mW/cm^2, the threshold voltage was 21 V. When the intensity increased to 3 mW/cm^2, there was a dramatic change in the threshold voltage. The threshold voltages measured at different intensities in Fig. 5.5(a) are plotted as a function of light intensity in Fig. 5.5(b). For intensities higher than approximately 3mW/cm^2, the threshold voltage saturated near the limit of the gate voltage scan, 100 V. In control experiments using FETs without the DR19 layer, there was no change in the threshold voltage under illumination.

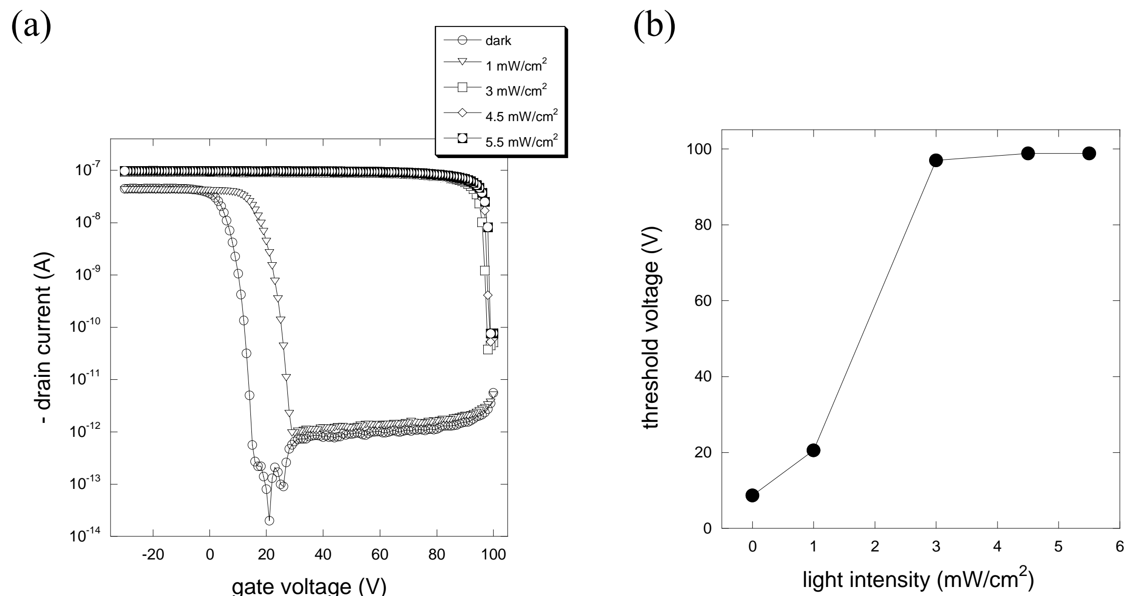

Fig. 5.5: (a) The effect of light intensity on the transfer characteristic curves of FET devices with DR19. The drain voltage was -5 V. (b) Threshold voltage as a function of light intensity.

5.6 Effect of gate electric field on threshold voltage shifts

The magnitude of the gate electric field during illumination plays an important role in determining the threshold voltage shift. The effect can be seen in Fig. 5.6. In the dark, the gate voltage was scanned from 50 V to -60 V for a sample in which a 30 nm pentacene film was deposited on DR19. A scan in the reverse direction from -60 V to 50 V was carried out under the same conditions. The threshold voltage during the scans in the dark was -43 V and -44 V, for the forward and reverse directions, respectively. This small difference between the threshold voltages measured for the two scan directions in the data shows that the effect of the gate voltage was negligible in the dark. When the device was illuminated, there was a large difference in the threshold voltage dependent on the scan

directions. In the scan from 50 V to -60 V, the threshold voltage was 3.5 V. In the opposite directions, the threshold voltage was -39 V.

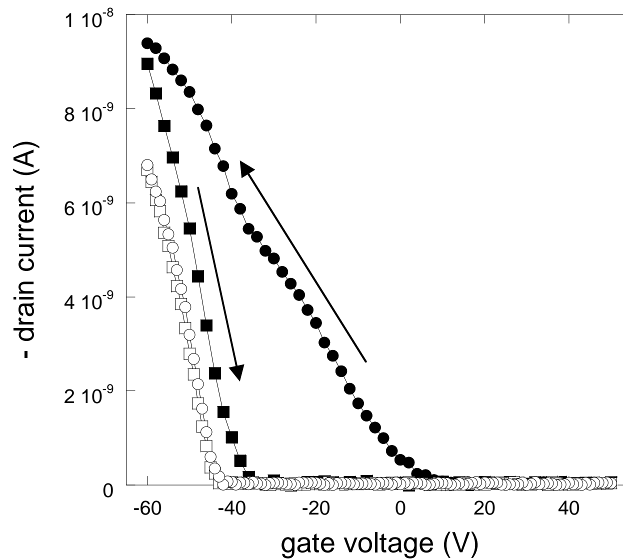

Fig. 5.6: Drain current-gate voltage characteristics in the linear regime with V_D=-2 V for a pentacene FET on a DR19 layer. The gate voltage was scanned from 50 V to -60 V (circles) and from -60 V to 50 V (squares) in the dark (open symbols) and under illumination (filled symbols).

5.7 Effect of the DR19 thickness on threshold voltage

The thickness of the DR19 layer on SiO_2 also changes the threshold voltage. By varying the solution deposition time of DR19 the surface coverage can be altered. The magnitude of the threshold voltage shift is plotted as a function of the deposition time of DR19 in toluene in Fig. 5.7.

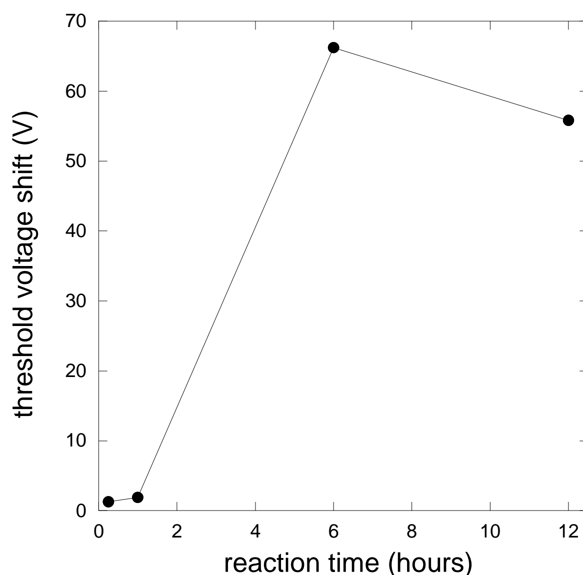

Fig. 5.7: Variation of the threshold voltage of pentacene FETs on DR19 as a function of the time for which the FET devices were exposed to the DR19 solution.

For deposition times of 1hour or less, the change in the threshold voltage was less than 10V. In 6 hours, the DR19 formed a thick layer resulting in the large shift from -12 V to +54 V upon illumination. The short deposition time less than 1 hour produces isolated DR19 islands with vacant sites between them where pentacene is directly deposited onto SiO_2 instead of DR19. It is speculated that pentacene deposited on DR19 has a higher concentration of holes than on SiO_2. When the area coverage of DR19 is not sufficient to form the conducting path no current flows between electrodes. The threshold voltage shift we observed arose from the changes in either DR19 or the interface between DR19 and pentacene, not from a change at the interface between pentacene and SiO_2 after the

reaction of the device in the DR19 solution. The threshold voltage shift was negligible in a control sample without DR19.

5.8 Structural changes in DR19 under illumination

One possible explanation for the large shift in the threshold voltage is a change in the dipole moment of the DR19 molecule under illumination. The magnitude of the dipole moment of the DR19 required to change the threshold voltage for the pentacene FET with the DR19 layer can be estimated using the description proposed by Kobayashi *et al*. [5]. The mobile charge carrier density induced (Q_{DR19}) in the pentacene layer deposited on the DR19 layer can be determined using the following equation:

$$Q_{DR19}=C_{ox}\Delta V_T= (\varepsilon_0\varepsilon_{ox}\Delta V_T)/(d_{ox}) \quad (5.1)$$

Here, ΔV_T is the shift in the threshold voltage of the pentacene transistor induced by the DR19. C_{ox} is the capacitance per unit area of the oxide and ε_0 and ε_{ox} represent the relative permittivities of free space and the oxide, respectively, and d_{ox} represents the thickness of the oxide. The mobile charge carrier density induced by the DR19 layer is also given by [6]:

$$Q_{DR19}=-C_{DR19}\Delta U= -(\varepsilon_0\varepsilon_{DR19}\Delta U)/(d_{DR19}) \quad (5.2)$$

Here, ΔU is the potential difference across the DR19 layer. C_{DR19} is the capacitance of the DR19 layer and ε_{DR19} represents the permittivity of DR19.

Thus, ΔV_T can be expressed using equation (5.1) and (5.2) by:

$$\Delta V_T= -(\varepsilon_{DR19}d_{ox}\Delta U)/(\varepsilon_{ox}d_{DR19}) \quad (5.3)$$

ΔU can be expressed by [6-9]:

$$\Delta U = -(\mu_{DR19})/(A_{DR19}\ \varepsilon_0\ \varepsilon_{DR19}) \tag{5.4}$$

Here, A_{DR19} is the area occupied by a DR19 molecule and μ_{DR19} is the dipole moment of the DR19 molecule. Based on equation (5.3) and (5.4), ΔV_T can be expressed by equation (5.5):

$$\Delta V_T = (\mu_{DR19} d_{ox})\ /(A_{DR19}\ \varepsilon_0 \varepsilon_{ox} d_{DR19}) \tag{5.5}$$

If we assume that DR19 is uniformly deposited on SiO_2 with a monolayer thickness of 2 nm, the dipole moment of a single DR19 molecule is 10 Debye and $1/A_{DR19}$ of DR19 is 10^{14} molecules/cm^2. The shift in the threshold voltage due to the DR19 Layer predicted by equation 5.5 is 96 V.

From the gate voltage-drain current characteristic curves performed in the dark, the magnitude of the shift in the threshold voltage of the pentacene FETs formed on the DR19 layer was less than 10V which is negligible. The difference is due to the fact that DR19 formed thick layers, more than 30 nm, and the large dipole moment of the DR19 molecules in the layer is averaged to nearly zero by the disorder in the thick films of DR19.

During illumination, however, the DR19 molecules in the thick film can be reconfigured and the net dipole moment of the DR19 can increase. The magnitude of the polarization required to observe the large shift of 100 V found in Fig. 5.4(b) during illumination can be estimated. The polarization of the layer is expressed by:

$$P = (\varepsilon_{DR19} \Delta V_T)/(\ d_{DR19} + d_{ox}) \tag{5.6}$$

We do not have information about the dielectric constant of DR19 films. Here, we assumed that $\varepsilon_{DR19} = 5\varepsilon_0$. When the change in the threshold voltage due to the DR19 layer is

100 V, the polarization of the DR19 layer is 1.9×10^{-6} C/cm^2. The mean net dipole moment per molecule, P_{avg}, can be calculated from the following equation:

$$P=P_{avg}N \quad (5.7)$$

If we assume that the packing density of DR19 molecules is $N=10^{21}$/cm^3, the electric dipole moment per molecule is calculated based on equation 5.7 and a polarization of 1.9×10^{-6} C/cm^2. An electric dipole moment per molecule of 5.7 Debye is required to achieve a change in the threshold voltage of 100 V. This result supports that the DR19 layer can be temporarily polarized by the combination of the illumination and the applied electric field. The polarized DR19 layer can change the threshold voltage of the FET.

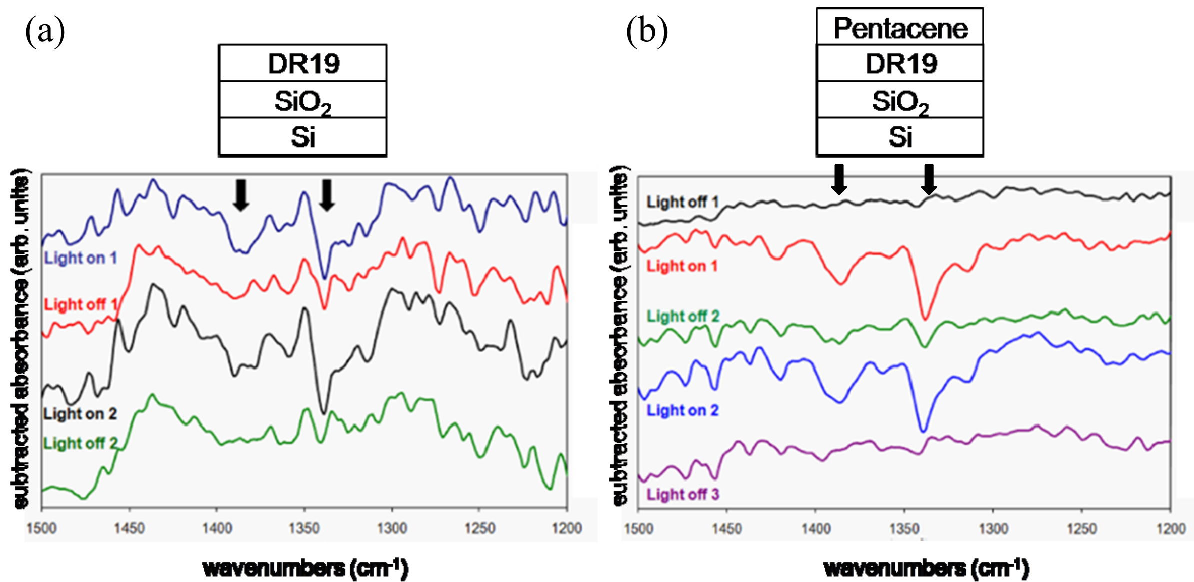

Fig. 5.8: ATR-FTIR spectra of (a) a DR19 layer on SiO_2 and (b) pentacene on the DR19 layer. The sequence of the spectra measured is from the top to bottom. A background spectrum of the DR19 layer was taken in the dark and subtracted from each spectrum. Two arrows indicate the reduction of the absorption at 1338 and 1384cm^{-1}.

We have found spectroscopic evidence for the changes in the DR19 layer during illumination. A charge-separated state of DR19 found under illumination can increase the dipole moment of DR19 from 10 Debye in the ground state to 20 Debye [10, 11]. The different configurations of the DR19 molecules in the two states can change the infrared absorption spectrum of the DR19 layer. The ATR-FTIR spectra from a DR19 layer with and without the pentacene layer are shown in Fig. 5.8(a) and (b). The spectra were acquired by subtracting the observed spectrum from the background spectrum measured in the dark.

When the DR19 layer was illuminated using a white light we observed a reduction in absorption at 1338 and 1384 cm^{-1} [4]. Those two peaks are assigned to the symmetric NO_2 stretch and N=N modes, respectively. The π-electrons of DR19 molecules are delocalized resulting in the charge-separated state of DR19 during illumination. The reduction of the absorption found in Fig. 5.8(a) under illumination indicates the charge-separated state occurred within the molecules. The reduced absorption at 1338 and 1384 cm^{-1} disappeared after turning off the light. These changes in the DR19 layers are consistent with a physical picture in which a net dipole moment of the DR19 film is assisted by internal reconfiguration in the chromophore, as has been previously suggested.

5.9 Photoinduced charge transfer between DR19 and pentacene

A second possible origin of the large shift in the threshold voltage of pentacene FETs on DR19 under illumination is trapping of electrons generated in the pentacene layer into DR19. Illuminating the pentacene layer creates electron-hole pairs. Applying a positive

gate voltage can cause the photogenerated electrons to transfer to the DR19 layer. This model is similar to photoinduced charge transfer at the interface between pentacene and C_{60} molecules as discussed in chapter 4. The trapped electrons in DR19 accumulates holes in pentacene layer near the interface. Therefore, the combination of the light and the gate electric field leads to the shift in threshold voltage.

5.10 Conclusions

The electrical method to characterize the change in the molecular conformation of photo-responsive molecules can be applied to a variety of applications such as optical sensors and organic photovoltaics. The reversible change in the structure of chromophores in response to light ensures that chromophores can be incorporated into light sensing devices. The chromophore can also be used as both electron donor and acceptor layers in molecular organic solar cells due to its polarizability under illumination.

The degree of reconfiguration of chromophores during illumination can be estimated by measuring the magnitude of the change in threshold voltage of OFETs. Our system can be used to evaluate the photosensitivity of chromophores.

5.11 References

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Chapter 6

Ambipolar Rubrene Thin Film Transistors

6.1 Introduction

Transistors have been fabricated from single crystals of the organic semiconductor. Rubrene ($C_{42}H_{28}$) has the highest mobilities of OFETs. Rubrene devices have mobilities up to 20 cm^2/Vs [1-3]. Podzorov studied transport of holes in the surface of rubrene single crystals using air-gap field effect technique [1]. Rubrene single crystals were placed on a polydimethylsiloxane stamp in which source, drain and gate electrodes are patterned. The rubrene crystal is isolated from gate electrodes by air to reduce the density of surface defects. A high mobility of holes in the rubrene up to 20 cm^2/Vs was obtained using a 4-probe measurement which eliminates the contact resistance between metal electrodes and organic semiconductors. The mobility was anisotropic and a lower temperature led to a higher mobility, which are signatures of intrinsic transport of holes in rubrene single crystals. Hall effect measurements were used to measure the Hall mobility in the bulk of a rubrene single crystal [2]. A Hall mobility of 10 cm^2/Vs was acquired at a charge density less than 10^{11} cm^{-2} in the rubrene single crystal.

The rubrene single crystals are not practical for large scale devices, however, because the sizes of single crystals are limited. The use of thin films for FETs is desirable because thin film transistors can be applied to flexible and large-area electronics using low-cost manufacturing.

We have studied the electrical properties of rubrene thin films on SiO_2 substrates. The structural properties of rubrene were investigated using atomic force microscopy (AFM), Fourier transform infrared spectroscopy (FT-IR) and X-ray diffraction (XRD). We have performed *in situ* electrical measurements to understand how morphology of rubrene islands can contribute to the channel formation.

Surprisingly, both electron and hole conduction in rubrene films were found in the rubrene thin film on SiO_2. Ambipolar characteristics have been observed in a rubrene single crystal FET with a hydroxyl-free gate dielectric [4]. Single crystal rubrene FETs fabricated on SiO_2 gate dielectric, however, exhibited only *p*-type conductivity.

6.2 Experimental methods

In our rubrene thin film transistors, the gate dielectric was a 200 nm-thick thermally grown SiO_2 layer on a Si substrate. We deposited rubrene while the substrate was at room temperature. The rubrene molecules were sublimed from a solid source. The rubrene was preheated overnight at an effusion cell at a temperature of 120 °C before the deposition. A bottom-contact FET structure was employed for *in situ* electrical characterization. The channel length was varied from 10 μm to 100 μm, and the channel width was 1 mm. For the source and drain contacts, 60 nm thick gold layers were evaporated on 10 nm thick Cr layers on SiO_2.

6.2.1 Structural identification of rubrene using FT-IR

The FT-IR spectrum in Fig. 6.1 confirms that rubrene molecules were deposited on the SiO_2 substrate without decomposition. The peaks in the range from 690 to 900 cm^{-1} arise

from the C-H bending bands (out of plane bending) [5]. The C=C stretching peaks appear between 1430 and 1650 cm^{-1} [5]. The C-H stretching bands of aromatic compounds are in the range of 3000 to 3100 cm^{-1} [5]. The spectra of rubrene thin films are consistent with those reported in rubrene single crystals [6].

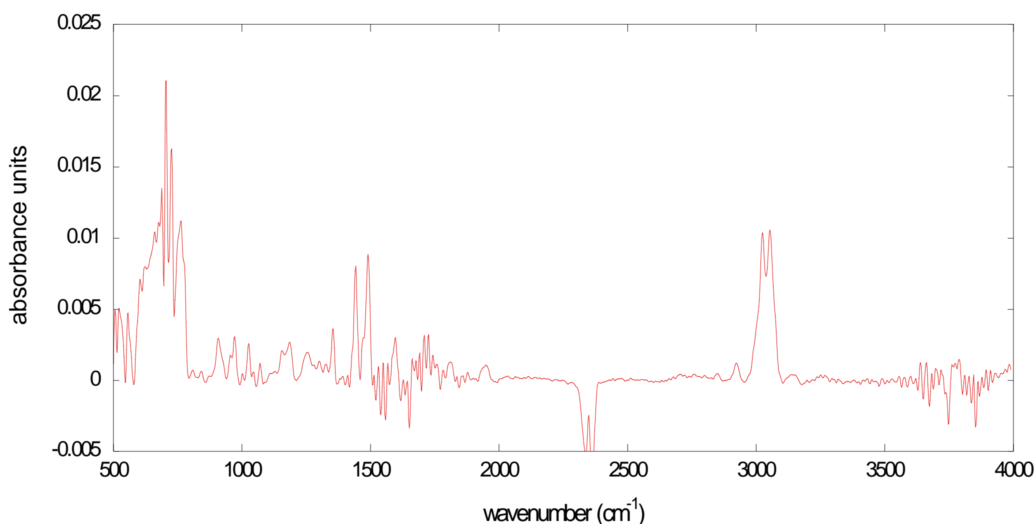

Fig. 6.1: FT-IR spectra of a rubrene thin film deposited on a SiO_2 surface.

6.2.2 3D growth of rubrene on SiO_2

When an organic material is grown on an inorganic surface, growth mode is determined by the relation between the surface energy and interfacial energy [7, 8]. If the surface energy of the inorganic surface is less than the sum of the surface energy of the organic material deposited and the interfacial energy between the organic material and the inorganic surface layer by layer growth occurs, and vice versa for island growth. Rubrene grows in three dimensional islands on SiO_2. The formation of rubrene islands on SiO_2 shows that the sum of the surface energy of rubrene and the interfacial energy between

rubrene and SiO_2 substrate is larger than the surface energy of SiO_2.

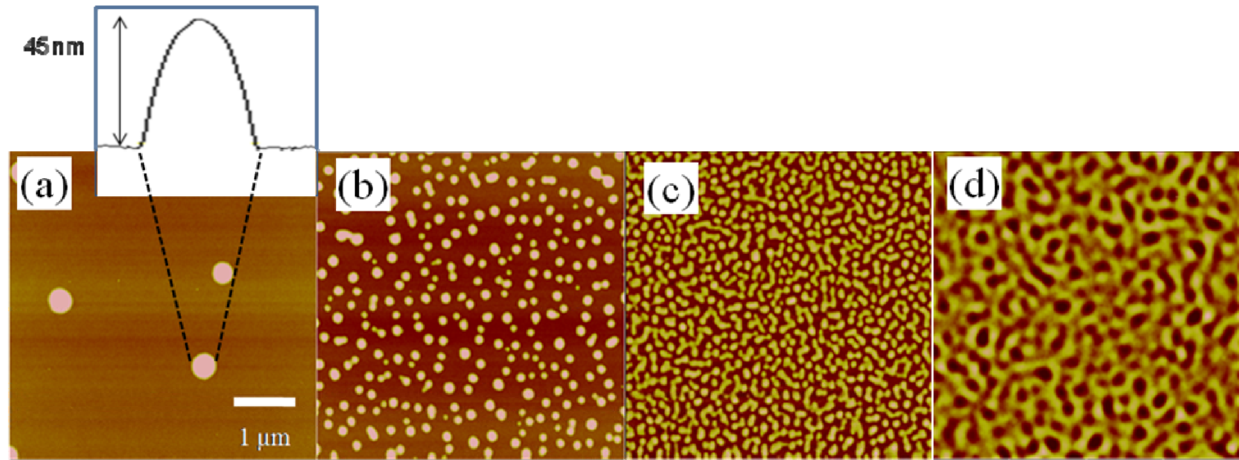

Fig. 6.2: AFM images of rubrene on SiO_2. After (a) 3 hours deposition with an effusion cell temperature of 186 °C. Inset shows the cross section of an island, (b) 30 min. deposition with an effusion cell temperature of 222 °C, (c) 25 min. at 240 °C, and (d) 8 hours 40 min. at 240 °C

Fig. 6.2 shows AFM images of rubrene islands deposited on SiO_2 at room temperature. A rubrene island on SiO_2 has a hemisphere shape as can be seen in the cross section of rubrene islands in the inset of Fig. 6.2(a). As the temperature at the effusion cell increases the number of islands per unit area increases (Fig. 6.2(a) and (b)). As the size of the islands increases, neighboring islands coalesce and form a two dimensional network as shown in Fig. 6.2(c). In very thick rubrene films, rubrene islands are connected with each other as seen in Fig. 6.2(d). The rms roughness of this surface is 6.8 nm. More rubrene added onto the SiO_2 surface leads to the rough surface. Rubrene islands grow in three dimensions up to heights of tens of nanometers. The contact angle of rubrene islands is 23° independent of

the size of rubrene islands.

6.2.3 Molecular orientation of rubrene on SiO_2

NEXAFS was used to study the orientation of molecules within the rubrene films on SiO_2. The total electron yield (TEY) is plotted as a function of photon energy in Fig. 6.3 for two different incident angles. The pronounced peak at 285.15 eV is due to excitations in the 4 phenyl side groups attached to the tetracene backbone of the rubrene molecules [9].

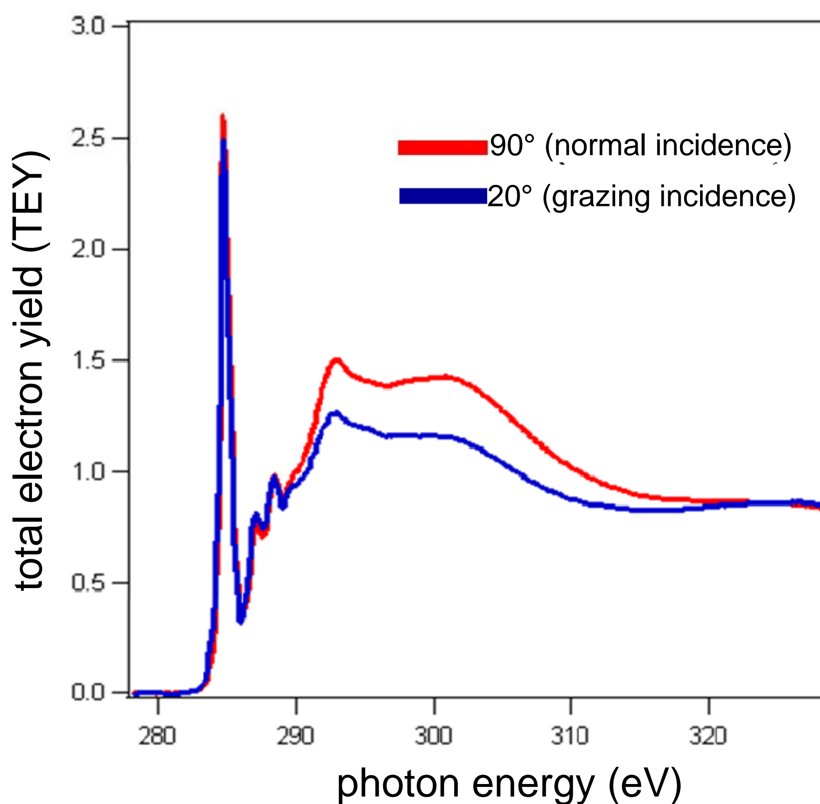

Fig. 6.3: C1s NEXAFS spectra of a thick rubrene film deposited on a SiO_2 substrate.

The intensity of the peak in TEY at 285.15 eV had little incident angle dependence, which shows rubrene molecules were randomly oriented on the substrate. In the literature, crystallinity of rubrene islands grown at room temperature on SiO_2 was investigated. Well-oriented crystalline rubrene films were obtained using hot wall deposition technique [10]. No evidence for the formation of crystalline grains was found with XPS and scanning electron microscopy (SEM) micrographs, which indicates amorphous films were formed on SiO_2.

6.3 Electrical properties of rubrene thin films

Charge transport in rubrene thin films was studied using bottom-contact FET devices. As demonstrated in chapter 2, the magnitude of the source-drain current in pentacene FETs is governed by the electrical properties of a few molecular layers close to the gate dielectric. Study of the formation of the conducting channel in rubrene is thus essential in probing charge transport in rubrene thin films. The shape and arrangement of the rubrene islands on SiO_2 is correlated with the formation of a conducting path in rubrene films.

6.3.1 Channel formation in rubrene thin film transistors

Fig. 6.5 shows the dependence of the source-drain current in a rubrene FET on the total amount of rubrene deposited on the SiO_2 substrate. As the thickness of rubrene increases, the drain current increases and then saturates. A rapid onset of current is observed at a rubrene thickness of approximately 5 nm.

The onset of current in Fig. 6.5 is due to the formation of the conducting path in rubrene films when the ratio of the area covered by rubrene islands to the total area in the channel

region is 0.67 based on the percolation threshold in a continuous two dimensional system [11]. This geometric percolation is based on the assumption that all rubrene islands have the same shape and size.

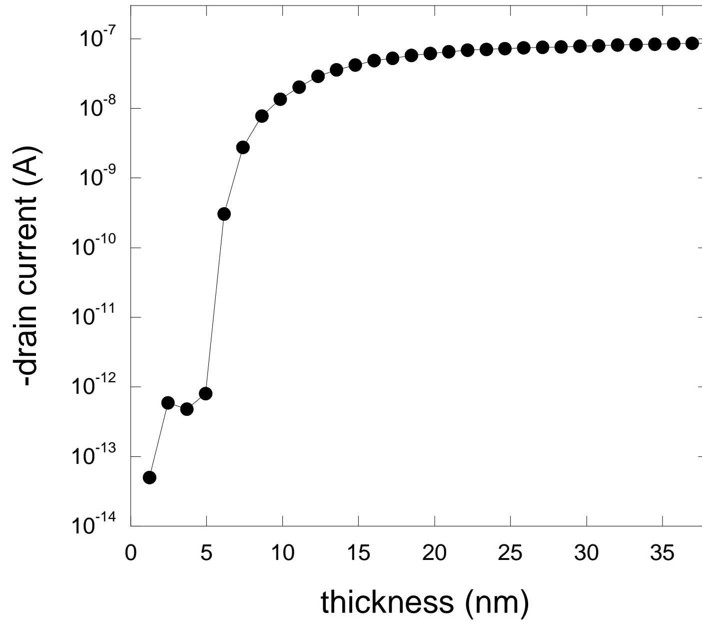

Fig. 6.5: Drain current as a function of the average thickness of a rubrene thin film. Each point was obtained at V_G=-70 V and V_D=-50 V. The deposition rate was 1 nm/min.

The average thickness of rubrene islands deposited was calculated in order to estimate the deposition rate at a particular effusion cell temperature (250°C). The total volume of rubrene islands deposited can be calculated based on the assumption that the rubrene islands are a spherical cap of radius *r*. The height of the cap is *h.* The volume of the spherical cap, *V*, can be expressed by:

$$V = \frac{1}{3}\pi h^2 (3r - h) \tag{6.1}$$

The radius of a spherical cap, r, is measured from the radius of the area on the surface that the rubrene island covers. The values of r and h can be measured from the AFM images of rubrene islands grown at the same effusion cell temperature as that used in the *in situ* electrical measurements of Fig. 6.5. The total volume of the rubrene islands deposited for 4 min was 2.4×10^7 nm^3 and the value was divided by the total area, 6.3×10^6 nm^2, where rubrene islands were grown, to calculate the average thickness of the rubrene islands. The deposition rate calculated was 0.96 nm/min at an effusion cell temperature of 250 °C.

The average thickness of rubrene at which the islands occupy 67 % of the channel area can be estimated from the number of rubrene islands and the volume of a rubrene island. When the ratio of the area covered by rubrene islands to the total area is 0.67, percolation between rubrene islands occurs [11]. The average thickness of rubrene at which percolation between islands occurs is obtained by dividing the total volume of rubrene islands at the percolation threshold by the total area of the AFM image we used for the measurement of r and h. We assumed that the number of islands is constant. The total volume at the percolation threshold was 3.1×10^7 nm^3 and this value was divided by the total area to estimate the average thickness of the rubrene islands at the percolation threshold. Based on the calculation, the current onset is predicted to occur at 5 nm. The current onset around 5 nm in our current-voltage characteristics is consistent with the predicted thickness at which the percolation should occur.

The mobility of holes in the saturation regime in rubrene thin films was less than 10^{-5} cm^2/Vs in repeated experiments. The very low mobilities arise from two factors. First, the

three dimensional growth of rubrene islands leads to poor connectivity between islands. Second, the rubrene thin films were amorphous leading to much lower mobilities for holes relative to those observed in rubrene single crystals. The NEXAFS results on rubrene films show that the rubrene molecules form amorphous films on the SiO_2 surface.

6.3.2 Ambipolar charge transport in rubrene thin films

Although the mobilities of holes in rubrene thin films are much lower than in single crystal transistors we also found that the transistors had ambipolar charge transport characteristics.

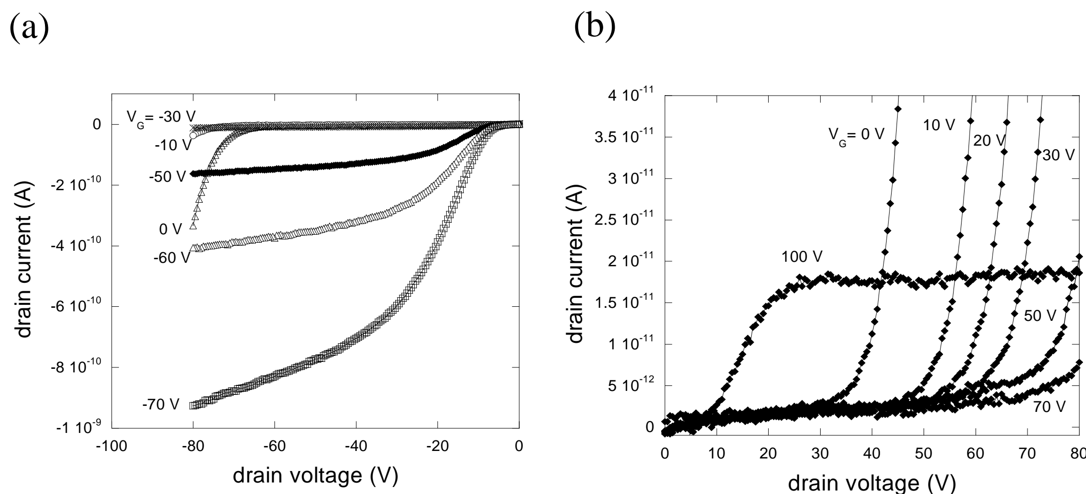

Fig. 6.6: Output characteristic curves of a rubrene thin film transistor. (a) p-channel operation. (b) n-channel operation.

The current-voltage characteristics of a rubrene transistor are shown in Fig. 6.6 and Fig. 6.7. The source and drain electrodes consist of a 60 nm Au film on a 10 nm Cr layer. These characteristics show that rubrene thin films grown on a SiO_2 substrate can transport both holes and electrons. As shown in the output characteristics in Fig. 6.6, abrupt increase in

drain current was observed for gate voltages between 0 and -30 V. This increase is due to electron current. At V_G=0 V the electron current begins to increase at V_D=-65 V. When a gate voltage of -10 V is applied, a drain voltage of -75 V is required to see the electron current. The electron current increased with larger negative drain voltage because more positive gate voltage than drain voltage increases the portion of electron accumulation layer relative to the hole accumulation layer in the rubrene channel. At more negative gate voltages than -30 V, the electron current disappeared for the drain voltages between 0 and -80 V and the device exhibited only conduction due to holes.

In the curves shown in Fig. 6.6(b), the drain voltage was scanned from 0 V to 100 V for several gate voltages. At V_G=100 V, the drain-source current increased and saturated with the increase of drain voltage, which is typical of FETs at electron enhancement mode. For the gate voltages less than 70 V, the current due to hole injection was observed for drain voltages more than 30 V.

The mobility in the saturation regime and the threshold voltages for n-channel and p-channel operations can be extracted from Fig. 6.7. In Fig. 6.7(a), the drain current increased as the gate voltage increased at positive gate voltages due to electron current (Fig. 6.7(a)). A more negative voltage increased the drain current due to induced holes in the channel (Fig. 6.7(b)). The hole mobility in the saturation regime was 6×10^{-6} cm^2/Vs and the threshold voltage was -35 V. As we make the gate voltage more positive, the hole current decreases and electron current increases for gate voltages above 70 V as in Fig. 6.7(b). The threshold voltage for electrons was +72 V and the mobility of electrons was 2.2×10^{-6} cm^2/Vs.

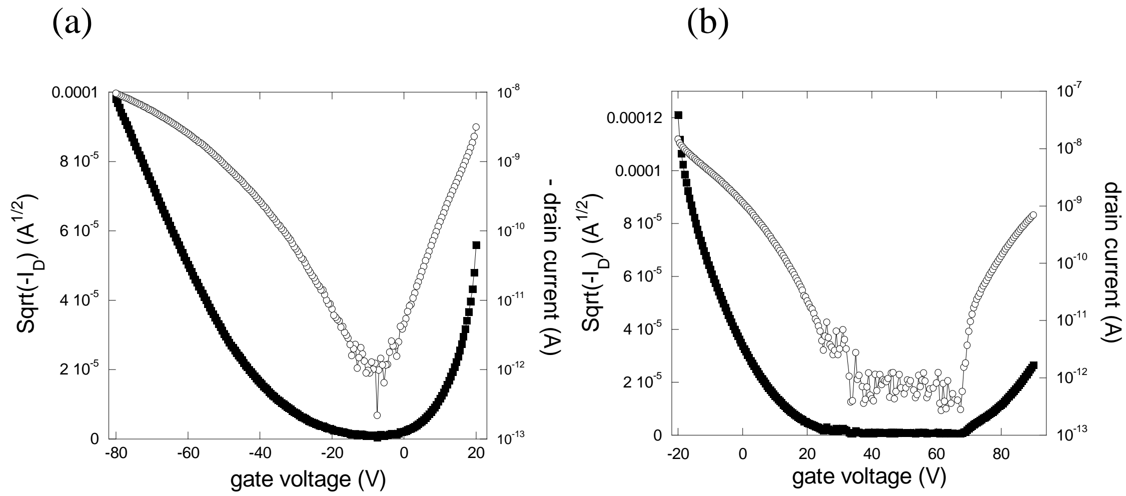

Fig. 6.7: Transfer characteristic curves of the rubrene thin film transistor. (a) Gate voltage scan from 20 V to -80 V at V_D=-70 V. (b) Gate voltage scan from -20 V to 90 V at V_D=70 V.

Using a value for the Schottky barrier based on the Schottky-Mott rule and the band alignment proposed by Hamada *et al.* [12], the difference in the magnitude of the current between Au and Cr for rubrene can be estimated. Under the assumption that charge injection from metal to semiconductor results from thermionic emission, the current density of a metal-semiconductor can be expressed by [13]:

$$J = A^{*}T^{2}\exp(-\frac{q\phi_{B}}{kT})(\exp(\frac{qV}{kT})-1) \tag{6.2}$$

Here, J is current density and A^{*} is Richardson's constant [13]. ϕ_B represents the barrier height and V is the applied voltage. Based on equation 6.2, the thermionic electron current between a Cr contact and rubrene would be a factor of 10^8 larger than with an Au contact. The contact area between Cr and rubrene is thus critical in determining the magnitude of

the current. The small contact area between 1 nm thick Cr and rubrene caused either no electron injection to rubrene or very small amount of curret, if any, in comparison with a 40 nm thick Cr layer.

The origin of ambipolar behavior in OFETs is not well understood [18]. One of the challenges in fabricating ambipolar transistors is to make charge injection of both electrons and holes into organic semiconductors possible. When the highest occupied molecular orbital (HOMO) level of organic semiconductors is at higher energy than the work function of electrodes, hole injection from organic semiconductors to the electrodes becomes favorable based on the Schottky-Mott rule. For electron injection, the lowest unoccupied molecular orbital (LUMO) level of organic semiconductors must be energetically below the work function of the electrodes. Yasuda *et al*. demonstrated that ambipolar transport in pentacene can be observed by reducing the electron injection barrier [14]. They used Ca electrodes with a low work function of 2.9 eV to see the conduction of electrons in pentacene.

The other challenge is the trapping of injected charges at the interface between gate dielectric and organic semiconductors. Chua *et al*. showed that the trapping of electrons injected at hydroxyl groups at the surface of the SiO_2 gate dielectric prevents ambipolar transport in organic semiconductors [15]. The concentration of hydroxyl groups at the surface of SiO_2 is in the range between 10^{13} cm^{-2} and 10^{14} cm^{-2}. This concentration is comparable to the carrier density of 10^{13} cm^{-2} in a FET operating at V_G=100 V.

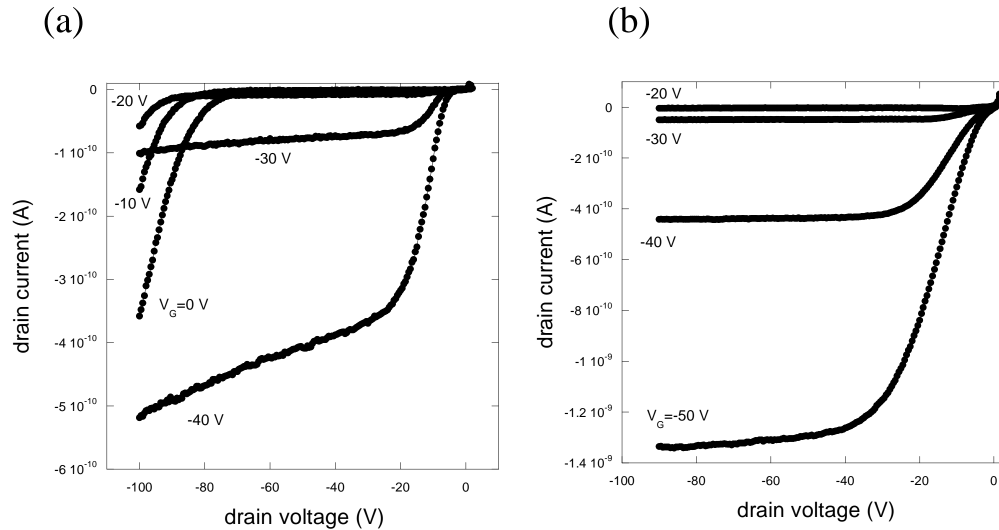

Fig. 6.8: Output characteristic curves of rubrene FETs with electrodes of (a) Au (50 nm)/Cr (40 nm) and (b) Au (50 nm)/Cr (1 nm).

Here, we studied the effect of the magnitude of the energetic charge injection barrier on the electron transport. We hypothesized that the ambipolar behavior in our rubrene thin film transistor is linked to a reduced electron injection barrier due to an electrode with a low work function. The 10 nm Cr adhesion layer of the source and drain electrodes made the charge injection of electrons possible because of the low work function of 4.5 eV. The highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) of rubrene are 5.36 and 3.15 eV below the vacuum, respectively [12]. A higher work function of the metal electrode can lead to a smaller barrier for hole injection from the metal electrode to HOMO level of rubrene. A lower work function of the metal electrode is better for electron injection into the LUMO level of rubrene. The lower work function of Cr, 4.5 eV compared with 5.1 eV of Au is more favorable to electron injection

to rubrene.

The role of the Cr adhesion layer can be further understood by using Au electrodes without Cr adhension layer. Two sets of electrodes were patterned on SiO_2. One is with source and drain electrodes using Au layers on 40 nm Cr layers and the other is with the same thickness and only differ in the thickness of Cr (1nm). For the device with the 40 nm Cr adhesion layer, ambipolar behavior was observed, as shown in Fig. 6.8(a). In contrast, no electron current was observed with 1 nm thick Cr layer (Fig. 6.8(b)).

The ambipolar behavior of rubrene on SiO_2 disappeared after the devices were exposed to air. This phenomena was also observed in FETs based on C_{60} which is *n*-type organic semiconductor [16].

6.4 Conclusions

We demonstrated rubrene thin film transistors on SiO_2. The mobility in these devices was very low compared with rubrene single crystal transistors due to the undesirable growth mode for charge transport and disorder in rubrene films. However, the ambipolar characteristics can provide much flexibility in organic circuit design.

Electrical properties of rubrene thin films could be improved through the optimization of growth conditions and the modification of the interface between a gate dielectric and a rubrene film.

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Chapter 7

Enhanced Hole Mobility in

Ambipolar Rubrene Thin Film Transistors on Polystyrene

7.1 Introduction

The mobility of charge carriers in rubrene thin film transistors built on SiO_2 is 4 to 5 orders of magnitude smaller than the mobility of rubrene single crystals [1-3]. Seo *et al*. demonstrated a rubrene thin film transistor on SiO_2 and found ambipolar characteristics in the rubrene transistors. Electron and hole conduction were observed in the rubrene channel. The mobilities from the rubrene FET characteristics were 8×10^{-6} cm^2/Vs for holes and 2.2×10^{-6} cm^2/Vs for electrons [1]. Rubrene FETs with amorphous and crystalline channels were fabricated on SiO_2. A rubrene island grown on SiO_2 consists of crystalline disk covered by amorphous rubrene region. The mobility of holes in a crystalline rubrene disk grown on SiO_2 was 1.23×10^{-4} cm^2/Vs [3].

The low mobility of holes in rubrene thin films is due to poor crystallinity of rubrene films grown on SiO_2. In addition, the morphology of rubrene films is quite different from that of pentacene, which has far higher carrier mobility. Pentacene forms a two dimensional charge transport layer in contact with a SiO_2 surface [4, 5]. Rubrene forms three dimensional islands on the gate dielectric. These islands are not favorable for charge carrier transport because of the small area of contact between three dimensional islands .

There have been attempts in several research groups to improve the structure of rubrene thin films. In order to enhance the charge carrier mobility, a pentacene buffer layer was used between rubrene and gate dielectric [6]. Using the pentacene buffer layer, hole mobilities up to 0.6 cm^2/Vs have been found in rubrene thin film devices with a top contact transistor geometry. In a second study, rubrene was grown on SiO_2 functionalized with octadecyltrimethylsilane (OTS) at elevated temperatures with hole mobilities up to 2.5 cm^2/Vs [7]. Crystalline films were formed on the smooth pentacene layer and the OTS layer. The structure of the films was studied using x-ray diffraction [7].

Here, we demonstrate that the morphology of the rubrene film can be controlled using a polystyrene (PS) layer, resulting in changes in charge transport in rubrene films. The mobilities of holes in rubrene thin films on the PS layer spin coated on SiO_2 are related to the structural properties of rubrene. Rubrene films on this PS layer have a smooth surface because the PS layer lowers the energy of the gate insulator/rubrene interface. PS is very hydrophobic and has a smooth surface. The root-mean-square (rms) roughness of PS is small. Fritz *et al*. found a rms roughness of 2 Å in a PS layer on SiO_2 [8].

7.2 Experimental methods

Cr (1nm)/Au (60nm) electrodes were patterned on the SiO_2 surface using photolithography. The channel length of our FET devices was between 100 and 300 μm and the width was 1 mm. The FET devices were spincoated with 1 wt% PS in toluene at 4000 rpm for 1 min. The thickness of the PS layer was measured using ellipsometry. The recipe we used yielded a PS thickness of 30 nm.

(a) (b)

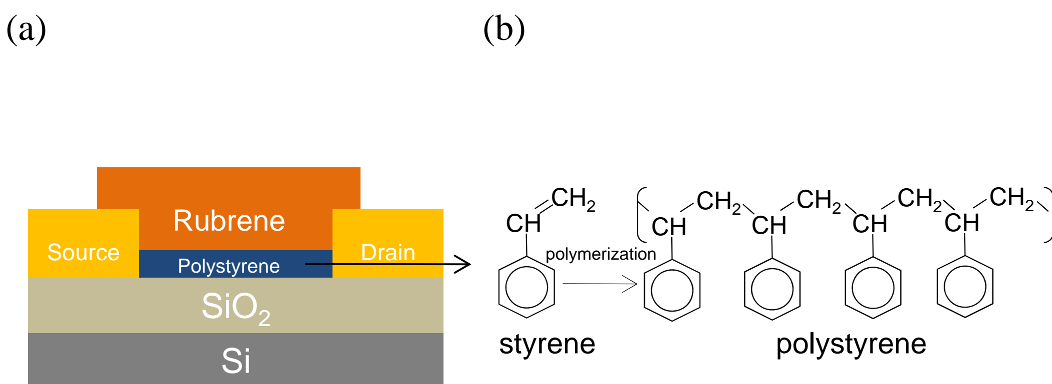

Fig. 7.1: Schematic digrams of (a) a rubrene transistor using a PS buffer layer and (b) the chemical structure of PS.

Rubrene thin films were deposited at the same effusion cell temperature (250 °C) used in the study of the rubrene channel formation in Chapter 6. We assumed that the deposition rate for these studies with PS layers is the same as it was for the same effusion cell temperature in our previous studies of rubrene on SiO_2. For all the rubrene depositions in this chapter, we used the same effusion cell temperature. Electrical measurements were done in vacuum at room temperature.

Fig. 7.2 shows an AFM image of a 30 nm thick PS layer on a SiO_2 surface. Randomly distributed pits arose from the poor wetting of the PS layer on the SiO_2 substrate [9]. The rms roughness of PS surface outside the pits was 0.3 nm. The contact angle was measured by using DI water on each different site of PS surface. The contact angle was 97.6 °. This shows PS has a hydrophobic surface which is consistent with values previously reported for a spin coated PS surface [10].

(a) (b)

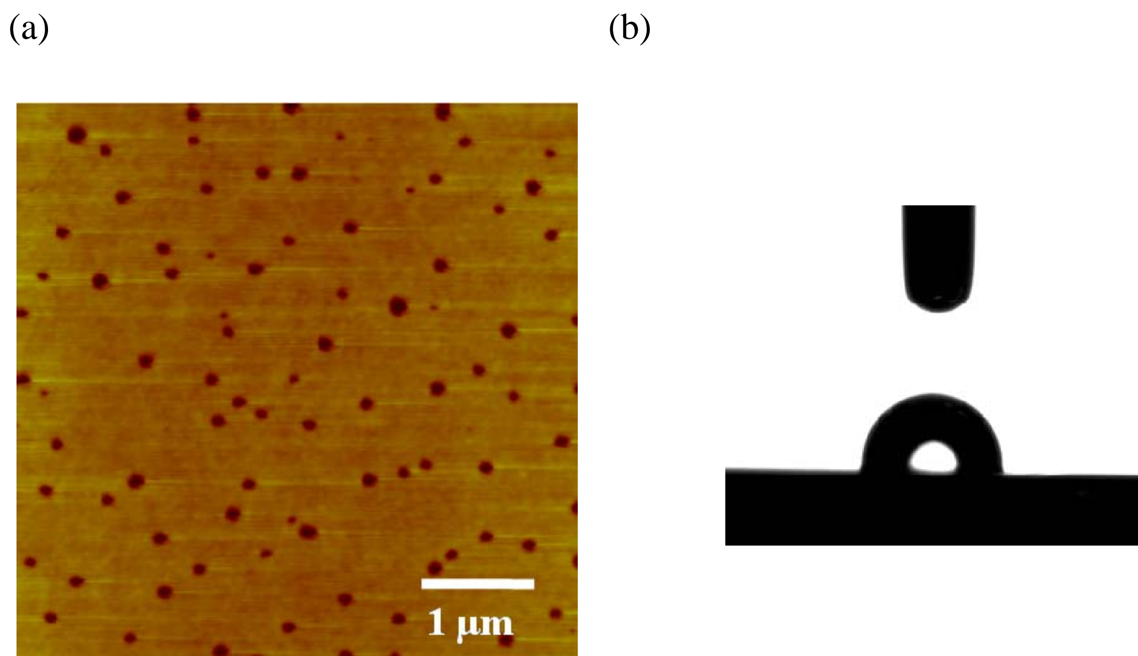

Fig. 7.2: (a) AFM image of a PS layer spin coated onto SiO_2. (b) A contact angle measurement using deionized (DI) water on PS.

7.3 Growth of rubrene on polystyrene

Fig. 7.3 shows rubrene films deposited on SiO_2 and PS surfaces. In the line scan in Fig. 7.3(a), the heights of the rubrene islands on SiO_2 are between 10 and 30 nm. In contrast to the morphology of rubrene films on SiO_2, rubrene films on PS formed smaller islands that complete a connected layer at a much smaller average thickness (Fig. 7.3(b)). On the PS layer, rubrene formed a continuous film, as suggested by the rms roughness of 0.98 nm, relative to the rubrene film on SiO_2. Rubrene islands contacted each other at a much earlier stage on the PS layer, then on SiO_2

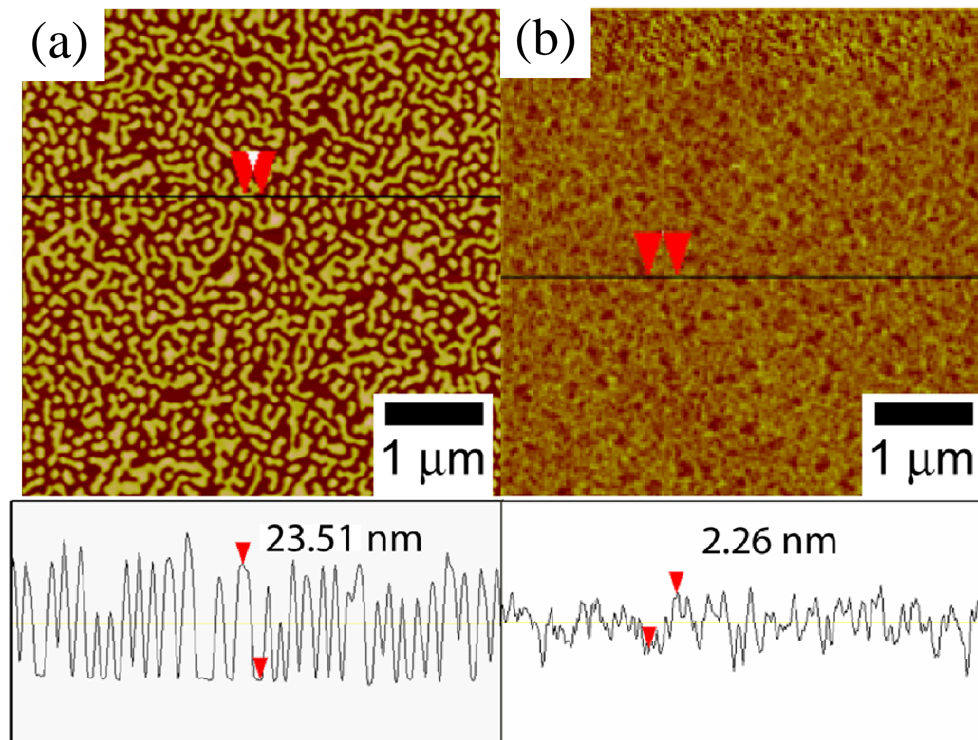

Fig. 7.3: AFM image of rubrene thin films on (a) SiO_2 and (b) PS. The difference in rubrene morphology between films on SiO_2 and polystyrene is visible in the cross sections plotted below (a) and (b).

7.4 Electrical properties of rubrene on PS

The morphology of the rubrene has a large effect on charge transport in FETs. Fig. 7.4 compares the mobility of rubrene films on a SiO_2 surface with that of rubrene on PS. In Fig. 7.4(a), the hole mobility was measured at the saturation regime where the mobility is determined from the linear fit in the plot of V_G versus $(-I_D)^{1/2}$. The mobility of holes in a rubrene thin film on SiO_2 was 6.8×10^{-5} cm^2/Vs, which is much lower than for rubrene single crystal transistors. The mobility of holes in rubrene thin film transistors fabricated on PS was 9.9×10^{-3} cm^2/Vs, which is two orders of magnitude larger than rubrene on SiO_2.

Seth King of Paul Lyman's group in Univ. of Wisconsin-Milwaukee did surface X-ray diffraction experiments for the rubrene films grown on PS and SiO_2 at the Argonne National Laboratory. The results showed no signs of crystalline X-ray reflections in rubrene films on both substrates.

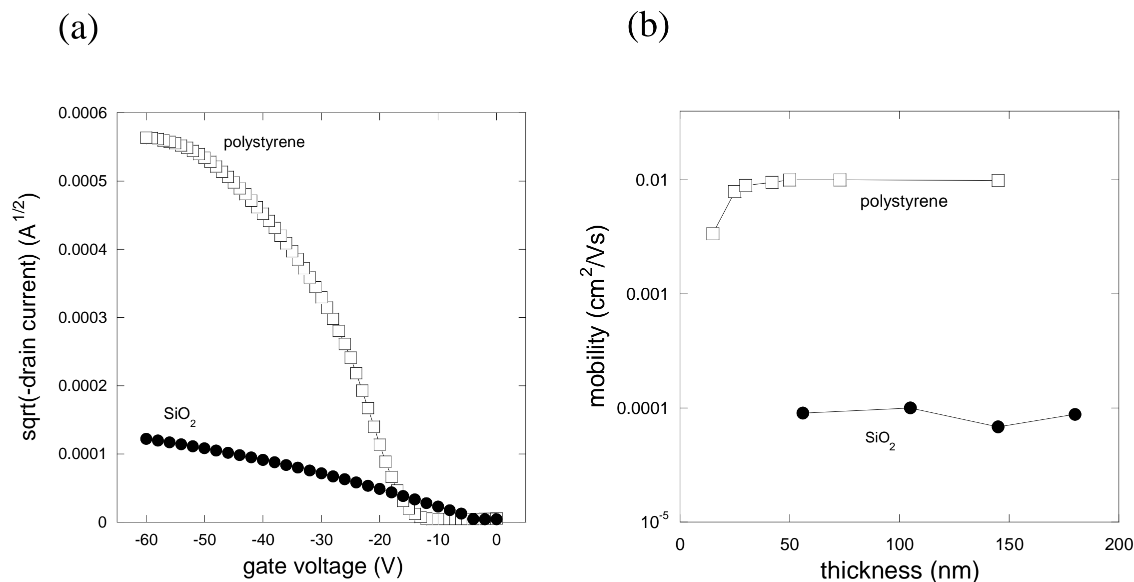

Fig. 7.4: Electrical properties of rubrene films on SiO_2 and PS. (a) Transfer characteristic curves for a 145 nm thick rubrene film (b) Hole mobility in the saturation regime as a function of thickness.

In Fig. 7.4(b), the mobility of holes is plotted as a function of rubrene thickness. After the percolation of rubrene islands, the mobility of holes did not increase as more rubrene was added to either PS or SiO_2 substrates. This led to the saturation of hole mobilities in rubrene films on both substrates after 50 nm on SiO_2 and 20 nm on PS. This saturation of the mobilities independent of the thickness shows the contacts between rubrene islands at a

small average thickness play a very important role in charge transport.

The large difference in the mobility of holes on SiO_2 and PS is due to the different morphology near the accumulation layer close to the gate dielectric. Rubrene on PS has larger contact areas between rubrene islands, decreasing the contact resistance between islands. Although the rubrene deposition continues, more molecules on the film did not contribute to the improvement of connectivity between rubrene islands.

7.5 Ambipolar characteristics of rubrene transistors

We found in Chapter 6 that the composition of the source and drain electrodes had a large effect on the transport of electrons in rubrene FETs. Fig. 7.5 shows transfer characteristic curves of rubrene FETs on PS at drain voltages of -60 V and 60 V for p-channel and n-channel operations, respectively. In Fig. 7.5(a), a hole current was observed at high negative gate voltages and increased with negative polarity of gate voltage. The electron current increased with positive polarity, which is typical for ambipolar FETs [11-13]. The threshold voltage for holes from the linear fit of V_G as a function of $-I_D^{1/2}$ in the saturation regime is -38 V. The onset of electron current occurred at a gate voltage V_G of -25 V. Fig. 7.5(b) shows n-type operations at the saturation regime. At high positive gate voltages, an electron current was observed. The threshold voltage for electron transport was 19 V. The hole and electron mobilities were 4.7×10^{-3} cm^2/Vs and 7.9×10^{-5} cm^2/Vs, respectively.

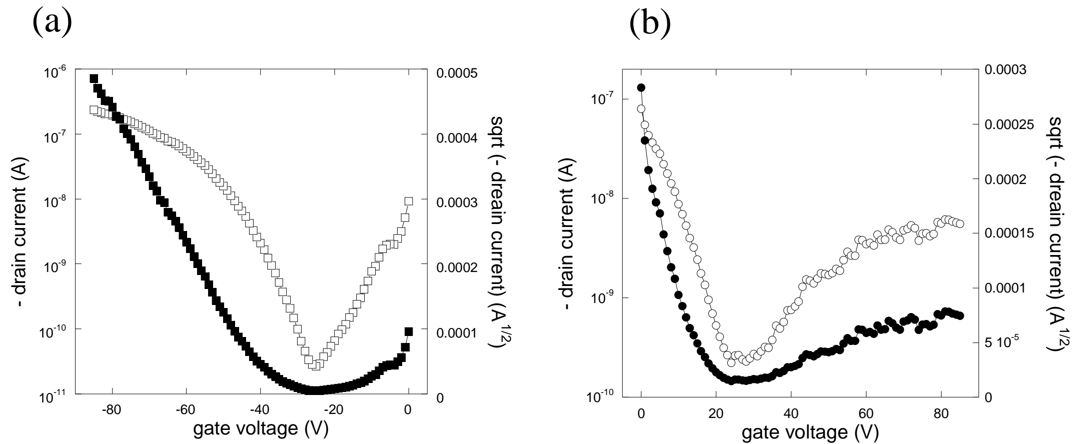

Fig. 7.5: Transfer characteristic curves of a rubrene FET formed on PS for (a) V_D=-60 V and (b) V_D=60 V.

As explained in Chapter 6, two phenomena are important in the conduction of both electrons and holes in organic semiconducting materials. One is electron transfer from metal electrodes to organic semiconductors and the other is trapping of electrons at the interface between gate dielectric and organic semiconductor. In Chapter 6, we found that the lower work function of Cr resulted in a lower barrier for the injection of electrons into rubrene films. The lowered barrier for electron injection from Cr layer to rubrene can not contribute to the conduction of electrons in rubrene thin films on PS because the 1 nm Cr adhesion layer is likely to be covered by the 30 nm PS layer. We believe that the electrons were injected from gold electrodes to rubrene layers on PS.

The electron current in rubrene films on PS could thus be due to the low trap density in the surface of the PS layer. A surface with higher trap density results in trapping more electrons and this requires the larger threshold voltage for n-channel operation by compensating the gate voltage applied. Although the electron current through gold

electrodes is much smaller than through Cr, the low trap density of PS for electrons makes it possible to observe the electron conduction in rubrene films. The SiOH concentration of ~4×10^{13} cm^{-2} on SiO_2 surfaces can lead to higher threshold voltage without PS. The evidence of the low trap density of PS is found in the low threshold voltage, 19 V, for electron current compared to values near 100 V obtained in rubrene FETs on SiO_2 without PS.

The low electron mobility in the rubrene FETs on PS is due to the poor electron injection from Au electrodes. The electron mobilities in these devices are comparable to those on SiO_2 even though the morphology of rubrene is more favorable to charge transport.

7.6 Conclusions

A more connected complete rubrene layer appears earlier in the deposition process due to the low interfacial energy between PS and rubrene films. This higher degree of connection results in enhanced hole mobilities in rubrene thin films. We also believe that this strategy can be applied to ambipolar heterojunction organic transistors that use double layers for hole and electron transport, such as a C_{60}/5,5´-bis(4-biphenylyl)-2,2´-bithiophene (BP2T) FET proposed by Yamane *et al*. [14]. In the device structures, the morphology of the layer close to gate dielectric can be manipulated to reduce structural disorder at the interface with a top layer.

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